Design Considerations of Differential Inductors In CMOS Technology for RFIC

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Abstract- Differential (symmetric) inductor is useful for its higher Q factor and smaller area than a single-end inductor in silicon-based RFIC. The limitations are the inductance value and the inductor track width. Large inductance or track width often results in too high of the overall capacitances and too large of the area. This paper addresses the issues of present differential inductor limitations and discusses a new type of differential inductor using multi-layer inter-leaf windings to overcome the present limitations. Significant area reduction is found. The designs based on the full-wave integral-equation simulation are intended for a six-metal layer 0.18μm CMOS technology, but it is also applicable to other silicon-base technologies. New compact high-performance differential inductors are fabricated and tested to validate the designs.

I. Introduction

Differential modes of operation have become the dominant choice in high-performance analog and mixed-signal circuits. In RFIC chip designs, the devices including inductors are used in pairs and placed symmetrically. It is possible to merge two symmetric inductors into a differential inductor [1-2]. One can treat a differential inductor as two single-end inductors inter-wound symmetrically. An example of the top view of a differential inductor is shown in Figure 1, where the windings are all in a common dielectric surface. A number of cross-under connections (as a bridge layer) are used to maintain geometric symmetry. The two inductors share the same flux area. For differential operation, the flux due to the inductor stretched from Port 1 to the center-tap would add to the flux of the inductor stretched from Port 2 to the center-tap. Effectively, differential inductor reduces the required inductor central empty area by half. Another significant advantage of differential inductors is the Q-factor enhancement as mentioned [1-2]. The Q factor can increase significantly (up to 50%) due to the reduction in the substrate resistance and the increase in magnetic flux. A important feature of the present differential inductors is that all the inductor windings are on the top metal layer where in CMOS technology, the metal thickness is much larger than the lower metal layers. This feature has the advantage of lower series resistance (higher Q). The problem is that the inductor windings need to expand laterally to increase the inductance or the track width. As a result, the edge-coupled fringing capacitance and the substrate parallel plate capacitance may be too large, the self resonant frequency may be too low, or the inductor layout is too large to be useful.

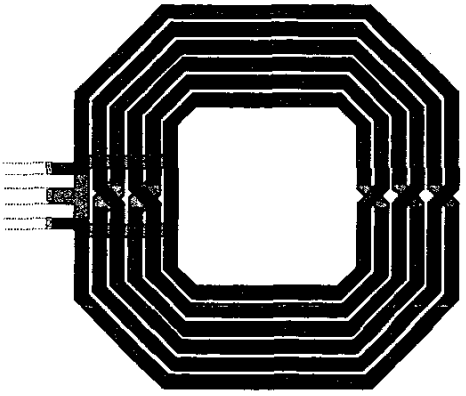

Figure 1. Top view of a six-turn differential inductor.

In this paper, we discuss the design limitations of the present differential inductors, in terms of the maximum inductor value, track width (important for Q factor and power handling), as well as the overall area for the 0.18μm CMOS 6-metal layer technology with a 2μm top metal layer and 0.53 μm lower metal layers. The designs should also be applicable to other similar CMOS technology with minor

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modifications. A new type of differential inductor utilizing multi-layer inter-leaf windings is proposed. The new inductor in series connection to lower metal layers, while remains symmetry, could significantly extend the limit of inductor value and track width, while reducing the overall size. The design is based on Zeland IE3D full-wave simulator. Several high-performance differential inductors are fabricated and test to demonstrate the design concept.

II. Design Considerations and Examples

In practice, for differential inductors, several identical windings in the lower metal layers are in shunt with the top metal layer to provide better Q at the cost of slight decrease of inductance and increase in capacitance. For simplicity, our discussion here is for inductors with a top metal layer only (except the bridge layers underneath). For the case in Figure 1, the equivalent circuit under differential operations (port 1 and port 2 voltage and current are 180 degrees out of phase) is shown in Figure 2 and the simulation results based on IE3D software are shown in Table I for several inductor values.

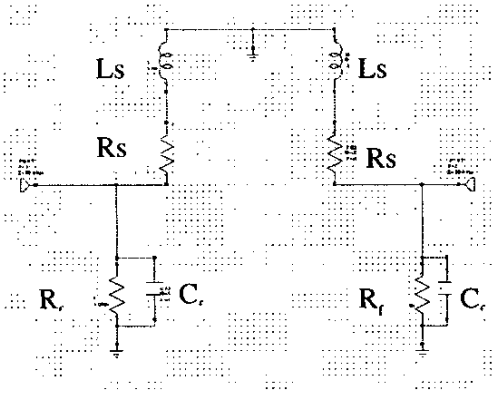

Figure 2. Equivalent circuit of a center-tapped symmetric inductor under a differential operation.

The example is for track width 10μm and track gap 2.8μm. The table shows that higher the inductance corresponds to larger ODM (outer dimension), and capacitance, and the self-resonant frequency. In usual circuit operation, one would like to have the inductor self resonant frequency at least twice the operating frequency for linearity and stability purpose. This sets up an upper limit of the inductor value one can use for a specific device frequency. The required inductor area (ODM), which is direct related to the chip die size and overall cost, is an important design consideration. Ideally, one would like to keep the inductor size as small as possible without losing the performance. In general, decrease the track width and increase the number of turns will decrease the size (not too much of the self-resonant frequency) at the cost of Q factor. The power handling may become an issue if the track width is too small. In general, an inductor value of 11~12nH is found the upper limit of a differential inductor for the 2.4GHz ISM band. For the given example, the inductor ODM of about 400μm for 8~9nH is too large and the resonant frequency too low for practical implementation.

Table I. Circuit parameters for a 6-turn differential inductor shown in Figure 1

ODM(μm)	272	334	386	430
Ls (nH)	4.84	7.26	8.47	11.0
Cf (fF)	179	220	254	283
Fr (GHz)	5.4	4.0	3.4	2.8

For the VCO tuning inductors, the demanding requirement on the Q factor (large track width) further limits the inductance. For 0.18μm CMOS technology with a 2μm thick top metal layer, Q of about 18 at 4GHz can be obtained using hexagon-shape windings and the multiple shunting on the lower metal layers. In this work, we demonstrate two high Q differential inductors, 2.1nH with four-turn 25μm track and 0.5nH with two-turn 25μm track.

Several differential inductors are fabricated and tested to validate the design principles. The measurements are performed with GSG 100μm probes on a probe station connected to a network analyzer up to 10 GHz. The measured two-port S-parameters are imported into Microwave Office Software to curve fit the equivalent circuit parameters. The effect of pads and traces used for

measurements are de-embedded from a separate pad open and short circuit measurement.

Table II, III, and IV show the comparison of measurement and simulation for three inductors, 6-turns 272μm, 4 turns 372μm, and 2 turns 256μm, respectively. Fairly good agreements are found. The discrepancy in capacitance is mostly due to the difference in the reference ground.

Table II. Measurement and simulation results for a 6-turn differential inductor in Figure 1.

272μm ODM, 6-Turns	Ls (nH)	Rs (Ω)	Cf (fF)	Rf (Ω)	Fr (GHz)	Q, 1GHz
Simulation	4.84	3.8	179	5300	5.4	7.6
Measurement	4.86	3.5	201	3450	5.1	8.1

Table III. Circuit parameters of a high-Q 2.1nH differential inductor for VCO

372μm ODM, 4-Turns	Ls (nH)	Rs (Ω)	Cf (fF)	Rf (Ω)	Fr (GHz)	Q 4GHz
Simulation	2.15	1.3	183	1450	8	17
Measurement	2.13	1.6	201	2100	7.7	18

Table IV. Circuit parameters of a high-Q 0.5nH differential inductor for VCO

256μm ODM, 2-Turns	Ls (nH)	Rs(Ω)	Cf (fF)	Rf (Ω)	Q 4GHz
Simulation	0.52	0.58	18	1220	18
Measurement	0.53	0.61	10	770	16

III. A New Layout of Differential Inductors

Power amplifier designs often require a large inductor value with a wide track to handle the required power. This requirement results in the inductor that is often too large if the metal windings are all on the top thick metal layer. The ODM formula is given as

$$\text{ODM} \approx l_{in} + 2N \times W + 2(N-1) \times S \quad , \qquad (1)$$

where l_{in} is the length of the inductor inner space, N: the number of turns, W: the track width, and S: the track gap. The increase of turns will reduce l_{in}, but the ODM will not vary much as seen in (1). For example, a 5nH (looking from each port) and 25μm track differential inductor requires an ODM over 480μm with 6 turns. This ODM is too large for practical purpose.

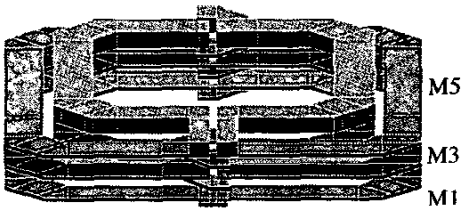

Figure 3. A new differential inductor layout using multi-layer winding.

Multi-layer spiral inductors are widely known and had been used extensively in RFIC chip designs [3-4]. The windings are stacked on top of each other in a multi-layer structure. The bottom layer winding acts as a shield for all the upper layers, resulting in significant reduction in substrate and fringe capacitance. Since there are only one or two turns on each metal layer, the multi-layer inductors are much smaller in size with higher self resonant frequency. A drawback is higher series resistance and lower Q.

In this paper, a new layout shown in Figure 3 is proposed. The use of multiple metal layer windings for differential (symmetric) inductors is to split the windings into two and center-tap together on the lowest layer. If only one turn on each layer, the right half turn is connected to the left half turn of the next layer, while the left half turn connects to the right half turn of the next layer. Two inductors are in effect inter-winding together to form a symmetric inductor. The resulting differential inductor would not work, however, due to the fact that the winding right on top or on bottom of a metal track belongs to the other inductor. The resulting parallel-plate capacitance is too large rendering the inductor

useless. We propose an approach here to remedy this problem. The idea is to move the opposite inductor winding outward as shown in Figure 3. The smaller turns occupy the even metal layers (M6, M4, and M2) and the larger turns occupy the odd metal layers (M5, M3, and M1). Basically, the inner right-half turns and the outer left-half turns form one inductor and the inner left-half turns and the outer right-half turns form another inductor. Pushing odd layer inductor winding outward reduces significantly the overall capacitance, although increases slightly the ODM. From the layouts in Figures 1 and 3, we can see that the new inductor structure is obtained in effect by moving the 2nd turn (counting from inside) of Figure 1 down to M5, 3rd and 5th turns down and back right into the bottom of the 1st turn, and 4th and 6th turns down and back into the bottom of the 2nd turn.

Table V. Comparison of the differential inductors of a single-layer windings and multi-layer inter-windings.

	Simulation Multi-layer (Figure 3)	Measurement Multi-layer (Figure 3)	Simulation Single-layer (Figure 1)
Ls (nH)	5.09	5.39	4.94
Rs (Ω)	6.8	7.1	3.0
Cf(fF)	329	326	230
Rf(Ω)	1950	1537	1118
Fr (GHz)	3.9	3.8	4.7
Q, 1GHz	4.4	4.3	8.1

A 5nH differential inductor of 25μm track width is designed based on the layout of Figure 3. The ODM is 262μm. In comparison, it is found that if all 6 turns are on the top metal layers with the same track width, the ODM is about 480μm. Therefore, the use of multi-layer inter-windings results in a significant 75% reduction in the overall area. The comparison is shown in Table V together with the measured results for the new inductor. Fairly good agreement between measurement and simulation is found. The new inductor that uses the lower thinner metal layers has lower Q factor as expected. In the design, the inner and outer turns lateral gap spacing is 5μm. Increasing this lateral spacing will reduce the coupling capacitance of the two merged inductors. The self-resonant frequency of the multi-layer differential inductor could easily be comparable to or higher than the single-layer case. The new structure could be potentially very useful for chip size reduction.

IV. Conclusions

In this work, we investigated the limitations of single-layer differential inductors in silicon-based RFIC. The increase in inductance or the inductor track width may lead to too high of the overall capacitances or too large of the area. Examples were given to demonstrate the limitations. We also proposed a new type of differential inductor using multi-layer inter-leaf windings to overcome the size limitations. For a six-metal layer 0.18μm CMOS technology, we demonstrated with both simulation and measurement that with the same inductance and track width, the new multi-layer differential inductor could be 75% smaller than the single-layer one. This could reduce the chip size and cost significantly.

III. References

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