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Reversible Comparator Design Using Quantum Dot-Cellular Automata

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ABSTRACT

Quantum dot-cellular automata (QCA) emerge as a research area to design nanometre scale logic circuit. In digital logic design, a comparator is the fundamental building block that performs the comparison of two numbers. This paper deals with the design of reversible building block for 1-bit comparator and its implementation in QCA. An improved QCA layout of Feynman gate is also achieved. The QCA Feynman gate is denser and has low delay than the existing circuit. The proposed reversible comparator has quantum cost 9, whereas the QCA reversible comparator has the quantum cost 0.927. The quantum cost based comparison of the proposed QCA reversible comparator with conventional reversible comparator shows the cost effective circuit design in QCA. The simulation result matched the truth table of comparator which approves the functional capability of the proposed QCA layout of comparator. All the proposed layouts dissipate very low power.

KEYWORDS

Feynman gate; majority gate; QCA; reversible comparator; TR gate

1. Introduction

Heat energy dissipation and circuit density are the key parameters in designing digital logic circuit to perform nanocomputing. The energy dissipation produced by the irreversible logic circuits can be patched up using reversible logic circuits [1]. In irreversible computation, if one bit of the information is lost, generates heat energy dissipation as k_BTln2 joules, where k_B stands for Boltzmann's constant and T stands for absolute computing temperature [2, 3]. Very low heat dissipation in logic computing can be accomplished through reversible computing [3, 4]. Reversible logic circuit has wide spread functionality in nuclear magnetic resonance, quantum, and optical computing. Quantum dot-cellular automata (QCA) is an intensifying nanotechnology that has high circuit density, very fast operating speed, and extremely low heat energy consumption. QCA is a transistor-less technology, where the columbic relation between QCA cells creates the path of propagation of information through QCA wire [5–9]. In QCA, information is carried out based on the charge of an electron that resides within a QCA cell rather as electrical power like in conventional complementary metal–oxide–semiconductor (CMOS) circuits [10–13]. The increasing density in circuit fabrication caused excessive power dissipation. The ultra low power consumption of QCA circuit may have an emerging functionality in reversible logic circuit design. This paper illustrates an optimized design of reversible 1-bit comparator and its implementation in QCA.

The major contributions of this work are as follows:

(1) An improved QCA layout of Feynman gate and TR gate is proposed.
(2) An optimized design of reversible comparator using TR gate and Feynman gate is achieved.
(3) A new QCA building block for the proposed reversible comparator has been achieved. The QCA outline has quantum cost 0.927.
(4) The comparative study of the proposed reversible comparator in traditional approach and QCA approach in terms of quantum cost is explored. The comparison shows the cost-effective design of the proposed reversible circuit in QCA.
(5) Power dissipation of the proposed layouts is estimated.
(6) The proposed QCA circuit of comparator is tested and verified with the truth table of comparator which measures the functional effectiveness of the circuit.

This paper is prepared as follows. Section 2 illustrates motivation and the major contributions of the work. The design of the proposed reversible comparator and its QCA layout is illustrated in Section 3. Section 4 deals with simulation results and discussions. Finally, the conclusion is drawn in Section 5.

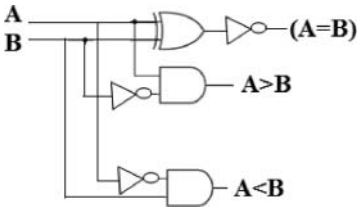

Figure 1: Logic circuit of 1-bit comparator.

2. Reversible comparator using QCA

2.1. Reversible logic circuit

A reversible logic circuit has a unique output for every input. Each input of reversible logic circuit can easily be estimated uniquely from its output. Inputs and outputs of any reversible circuit must be equal [1, 2, 14].

2.2. Comparator

A comparator is a combinational logic circuit that performs the comparison of two numbers and determines if one of them is equal to, greater than, or less than the other number [13, 14]. The comparison process is analogous to subtract micro-operation, apart from that the difference is not transmitted to a target register; only the status bits are affected. Let the two numbers be A and B. The truth table is in Table 1. Then, the output is specified by $A > B$, $A < B$, or $A = B$ as shown in Figure 1 and can be written as

$$F_{(A=B)} = (A'B + AB')' \tag{1}$$

$$F_{(A>B)} = A'B \tag{2}$$

$$F_{(A<B)} = AB' \tag{3}$$

2.3. Related work

An extensive literature on reversible comparator has been reported by the researchers. In this literature, a few of those are described through [15, 16]. An optimized design of 1-bit and 3-bit reversible comparators has been achieved in literature [15]. The reversible NG gate, DG gate, and Fredkin gate are utilized to design those comparators. The work in [16] describes the design and transistor implementation of reversible comparator circuit by using combination of several existing reversible gates such as Peres gate, Feynman gate, BJN gate, Toffoli gate, M gate, and L gate. However, this paper proposes an optimized design of reversible comparator than that of circuit proposed in [15, 16] and also outlines its QCA implementation.

Table 1: **Truth table of 1-bit comparator**

Input		Output		
A	B	$A > B$	$A < B$	$A = B$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

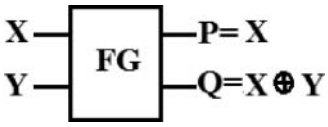

Figure 2: Block representation of Feynman gate.

2.4. Feynman gate

Feynman gate is a reversible logic gate that consists of two inputs and their corresponding outputs. The input bits (A, B) have one-to-one mapping function to output bits (P, Q) as described in Figure 2. Its quantum cost is measured as 1 [1–5]. The relevant truth table of Feynman gate is shown in Table 2.

The majority gate-based logic function of Feynman gate using Table 2 can be drawn as

$$P = X \tag{4}$$

$$Q = M\Big(M(X', Y, 0),\ M(X, Y', 0), 1\Big) \tag{5}$$

The equivalent QCA schematic and QCA layout are exposed in Figure 3(a) and 3(b), respectively.

2.5. TR gate

TR gate is a new reversible logic circuit that consists of three inputs and their corresponding unique outputs [17]. The input bits (A, B, C) have one-to-one mapping function to output bits (P, Q, R) as shown in Figure 4. Its quantum cost is calculated as 4 [17]. The appropriate truth table of TR gate is shown in Table 3.

Table 2: **Truth table of Feynman gate.**

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

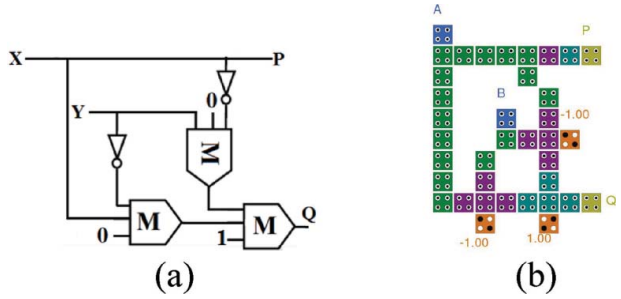

Figure 3: Feynman gate (a) QCA schematic, (b) QCA layout.

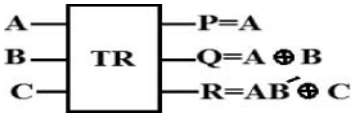

Figure 4: Block symbol of TR gate.

The majority gate-based logic equation of TR gate using Table 3 can be written as

$$P = A \tag{6}$$

$$Q = M\left(M(A', B, 0), M(A, B', 0), 1\right) \tag{7}$$

$$R = M\left(M\left(\left(M(A, B', 0)\right)', C, 0\right), M\left(M(A, B', 0), C', 0\right), 1\right) \tag{8}$$

The corresponding QCA schematic and QCA layout are exposed in Figure 5(a) and 5(b), respectively.

2.6. Design of reversible comparator circuit

By combining the functional property of TR gate and Feynman gate, the reversible 1-bit comparator can easily be achieved as shown in Figure 6. Only two TR gates and one Feynman gate are required to design the comparator. The proposed circuit generates only two garbage outputs.

Table 3: **Truth table of TR gate.**

Input			Output		
A	*B*	*C*	*P*	*Q*	*R*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

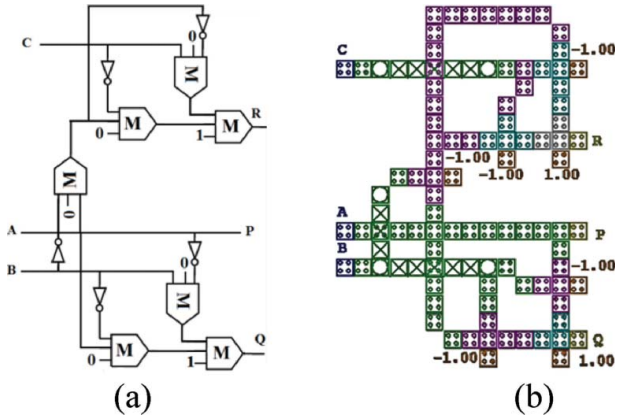

Figure 5: TR gate (a) QCA schematic, (b) QCA layout.

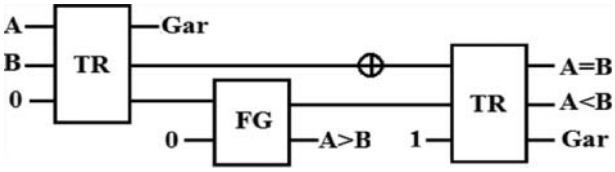

Figure 6: TR gate- and Feynman gate-based proposed reversible 1-bit comparator.

The logic equation corresponding to Figure 6 can be written as

$$\begin{aligned} F_{(A=B)} &= (A'B + AB')' \\ &= A \odot B \\ F_{(A>B)} &= (A'B \oplus 0) \oplus 0 \\ &= (A'B \oplus 0) \\ &= A'B \\ F_{(A<B)} &= (A \odot B \oplus A'B) \\ &= AB' \end{aligned}$$

The equivalent QCA schematic and QCA layout are shown in Figure 7(a) and 7(b), respectively.

3. Results and discussions

The design and simulation are achieved using bistable simulation tool, QCA Designer-2.0.3. The list of parameters used for bistable approximation is expressed in Figure 8. The size of the QCA cell is 18 x 18 nm.

Figure 9(a) shows the simulation output of Feynman gate achieved in QCA. The result is verified with theoretical knowledge prescribed in Table 2. For the input values $A = 0$ and $B = 0$, the output values will be $P = 0$ and $Q = 0$ as reflected in Figure 9(a). For the input values $A = 0$ and $B = 1$, the output values will be $P = 0$ and $Q = 1$ and so on. Figure 9(b) shows the simulation output

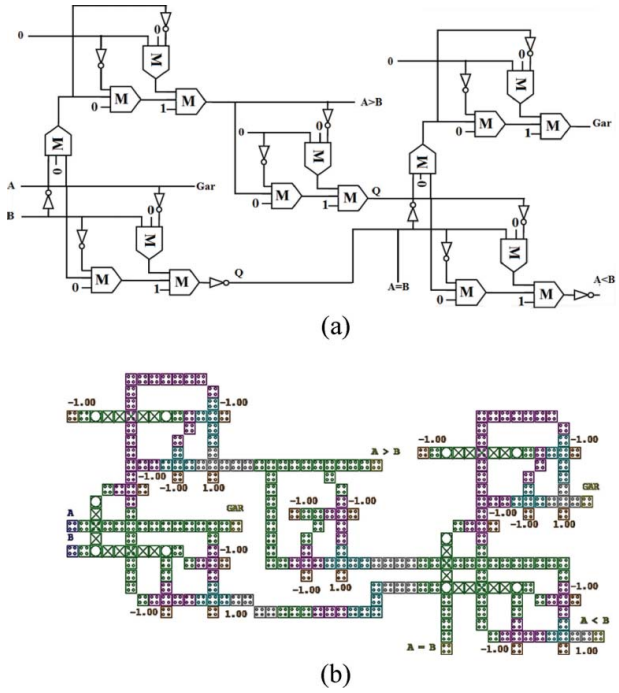

Figure 7: Proposed Feynman gate- and TR gate-based reversible 1-bit comparator (a) QCA schematic, (b) QCA layout.

Number Of Samples:	12800
Convergence Tolerance:	0.001000
Radius of Effect [nm]:	65.000000
Relative Permittivity:	12.900000
Clock High:	9.800000e-022
Clock Low:	3.800000e-023
Clock Shift:	0.000000e+000
Clock Amplitude Factor:	2.000000
Layer Separation:	11.500000
Maximum Iterations Per Sample:	10000

Figure 8: Bistable approximation parameter list.

of the proposed QCA layout of TR gate. The result is evaluated and verified with theoretical records as shown in Table 3. Figure 9(b) shows that for $A = 0$, $B = 0$, and $C = 0$, the output will be $P = 0$, $Q = 0$, and $R = 0$. For $A = 0$, $B = 0$, and $C = 1$, the output will be $P = 0$, $Q = 0$, and $R = 1$ and so on. The red arrow indicates the starting position of output R. Figure 9(c) deals with the simulation consequent of the proposed QCA reversible comparator. The result is compared and tested with theoretical value as shown in Table 1. The evaluation has

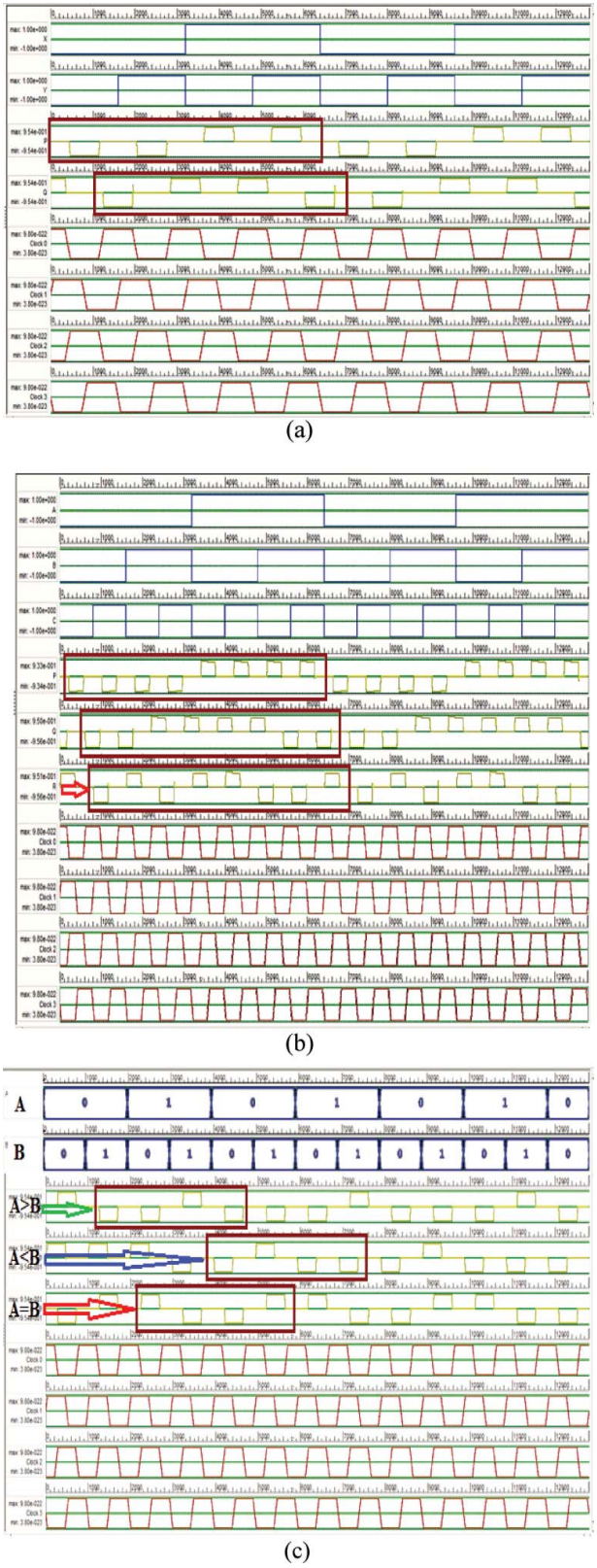

Figure 9: Simulation result of the proposed QCA circuit (a) Feynman gate, (b) TR gate, (c) 1-bit comparator.

acknowledged the efficiency of the proposed circuit. For inputs $A = 0$ and $B = 0$, the output values for $A > B$, $A < B$, and $A = B$ are 0, 0, and 1, respectively (Figure 9(c)).

Table 4: Circuit cost of the proposed reversible circuits

Proposed reversible circuit	Circuit cost
Feynman gate	1α
TR gate	$2\alpha + 1\beta + 1\gamma$
Proposed 1-bit comparator	$5\alpha + 2\beta + 3\gamma$

For inputs $A = 0$ and $B = 1$, the output values for $A > B$, $A < B$, and $A = B$ are 0, 1, and 0, respectively. The green, blue, and red arrows outline the starting point which is one, four, and two clock pulse delay for output bits $A > B$, $A < B$, and $A = B$, respectively. The outputs are shown by rectangle boxes.

3.1. Circuit cost and quantum cost of the proposed circuit

The number of AND operation, XOR operation, and NOT operation used to realize any reversible logic gate is considered as circuit cost for reversible circuit. The circuit costs of Feynman gate and TR gate are 1α and $2\alpha + 1\beta + 1\gamma$, respectively [18]; where α, β, and γ signify the number of XOR operation, AND operation, and NOT operation, respectively. The proposed reversible 1-bit comparator circuit as shown in Figure 6 required only two TR gates, one Feynman gate, and one reversible NOT gate. Thus, the reversible comparator has circuit cost as $2 \times (2\alpha + 1\beta + 1\gamma) + 1\alpha + 1\gamma$, i.e., $5\alpha + 2\beta + 3\gamma$ and the quantum cost can be calculated as $9\ (2 \times 4 + 1 = 9)$ as shown in Tables 4 and 5, respectively. The corresponding quantum cost of QCA layout of the proposed comparator is estimated in Table 6.

Figure 10 illustrates the quantum cost required to implement the proposed comparator in conventional technology and in QCA-based technology. Figure 10 confirmed that the QCA-based design has lower quantum cost than conventional design.

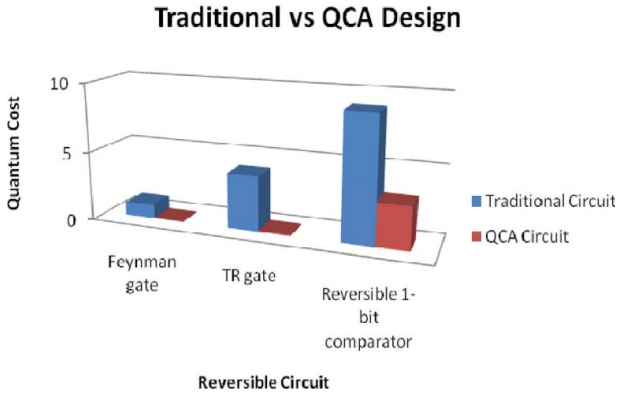

Figure 10. Quantum cost of the proposed conventional reversible comparator and QCA reversible comparator.

3.2. Complexity estimation of the proposed QCA circuit

Table 7 demonstrates the circuit complexity of the proposed design. The QCA circuit for Feynman gate required only 3 majority gates, 2 inverters, 46 QCA cells, 38,880 nm^2 total area, 14,904 nm^2 cell area, 38.33% area usages, and 3 clocking zones, whereas TR gate required only 7 majority gates, 5 inverters, 122 QCA cells, 90,720 nm^2 total area, 39,528 nm^2 cell area, 43.57% area usages, and 4 clocking zones. The QCA circuit for reversible 1-bit comparator is achieved by using 17 majority gates and 14 inverters. To design the comparator only 319 QCA cells are used that consumes 342,792 nm^2 total area, 103,356 nm^2 cell area, 30.15% area usages, and 4 clocking zones.

Table 5: Quantum cost of the proposed reversible circuits

Proposed reversible circuit	Reversible gate used	Quantum cost	Garbage output	Constant input
Feynman gate	–	1	–	–
TR gate	–	4	–	–
Proposed reversible 1-bit comparator	Two TR gates and one Feynman gate	9	2	3

Table 6: Quantum cost of QCA layout of the proposed reversible circuits

QCA layout of the proposed reversible circuit	Area (μm^2)	Latency (clock cycle)	Quantum Cost (area.Latency^2)
Feynman gate	0.023	0.75	0.013
TR gate	0.090	1.0	0.090
1-bit comparator	0.343	3.0	3.087

Table 7: Complexity of the proposed QCA circuit

Proposed QCA circuit	No. of majority gates	QCA count	Total area (μm^2)	Cell area (μm^2)	Area usage (%)	Clocking zones
Feynman gate	3 MVs and 2 inverters	37	0.023	0.012	52.17	3
TR gate	7 MVs and 5 inverters	122	0.090	0.039	43.57	4
Reversible comparator	17 MVs and 14 inverters	319	0.343	0.103	30.15	4

Note. MV: majority voter.

Table 8: Comparison of the proposed QCA Feynman gate circuit with the existing layout

QCA circuit of Feynman gate	Cell count	Area (μm^2)	Delay (clock cycle)
Proposed	37	0.023	0.75
Existing [19]	65	0.09	1.0
Improvement (%)	43.07	74.44	25

3.3. Comparison of the proposed QCA Feynman gate circuit with the existing circuit

Table 8 explores the comparison of the proposed QCA circuit of Feynman gate with the existing one reported in [19]. Table 8 illustrates that the circuit has an improvement of 43.07% in terms of QCA cell over existing layout. The circuit also has 74.44% and 25% improvement in terms of area and delay over [19], respectively.

3.4. Comparison of the proposed comparator circuit with the existing circuit

The proposed reversible 1-bit comparator has 18.18% and 30.86% improvement in terms of quantum cost over existing DG gate-based 1-bit comparator and NEW gate-based 1-bit comparator [15], respectively, whereas 43.75% and 10% improvement in terms of quantum cost over existing Toffoli gate-based 1-bit comparator and Peres gate-based 1-bit comparator [16], respectively. The design also has 60.82%, 57.13%, and 66.66% improvement over the existing one in [16] with respect to quantum cost, constant inputs, and garbage outputs, respectively, used in designing the circuit. The overall evaluation is shown in Table 9.

Table 9: Comparison of the proposed comparator with the existing circuit

Reversible 1-bit comparator	Quantum cost	Garbage value	Constant input
Proposed	9	2	3
DG gate-based design [15]	11	2	3
Improvement (%) w.r.t. [15]	18.18	Same	Same
NEW gate based design [15]	13	2	3
Improvement (%) w.r.t. [15]	30.86	Same	Same
Fredkin gate-based design [16]	23	6	7
Improvement (%) w.r.t. [16]	60.82	66.66	57.13
Toffoli gate-based design [16]	16	2	3
Improvement (%) w.r.t. [16]	43.75	Same	Same
Peres gate-based design[16]	10	2	3
Improvement (%) w.r.t. [16]	10	Same	Same

3.5. Power consumption by the proposed QCA layout of reversible comparator

Each QCA cell exhibits same power dissipation. During operation in one clock cycle, the power dissipation by the entire QCA circuit is estimated by considering the summation of power dissipation of all inverters as well as majority gates [7]. The procedure reported in [7] is utilized to estimate the power dissipation of the proposed QCA circuits at temperature $T = 2.0$ K in different tunnelling energy. The results are shown in Table 10 and explored through Figure 11. Here, T, E_k, and γ represent the operating temperature, kink energy, and tunnelling energy, respectively.

4. Conclusion

This paper outlines an advance design of Feynman gate and TR gate using QCA. The proposed QCA-based Feynman gate is denser and has low delay than the existing circuit. Quantum cost-effective reversible 1-bit conventional comparator is proposed and is realized in QCA. The proposed conventional reversible comparator is achieved with only two garbage outputs. The quantum cost and constant input of the proposed reversible comparator circuit are 9 and 3, respectively. The circuit has cost $5\alpha + 2\beta + 3\gamma$. The proposed QCA reversible comparator has high density 0.342 μm^2 area and the quantum cost is 0.927, which is optimized compared to traditional comparator. The comparative analysis with the existing comparator describes the cost-effective design of the proposed circuit in terms of quantum cost and garbage outputs. The reversible QCA comparator dissipated very low energy. Simulation result of QCA

Table 10: Power dissipation of the proposed reversible QCA circuits

Proposed QCA design	Dissipation of power at $T = 2.0$ K			
	$\gamma = 0.25E_k$ (meV)	$\gamma = 0.5E_k$ (meV)	$\gamma = 0.75E_k$ (meV)	$\gamma = 1.0E_k$ (meV)
Feynman gate	104.3	107.8	113.3	119.6
TR gate	319.1	327.8	342.5	359.6
Reversible 1-bit comparator	629.9	660.5	707.9	762.8

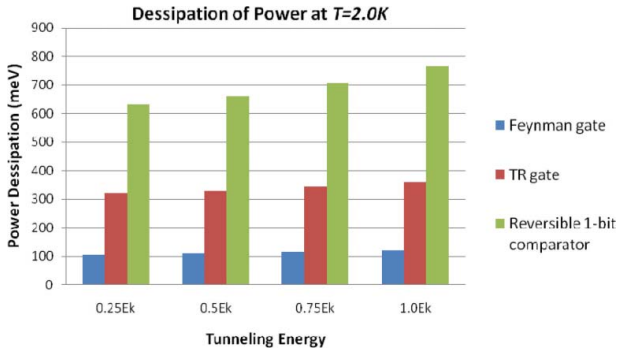

Figure 11: Power dissipation of the proposed QCA layouts.

circuit of the proposed reversible comparator is confirmed by comparing with the truth table that established the functional efficiency of the circuit. In near future, the proposed design can be used to achieve more complex reversible comparator like 2-bit, 3-bit, or even *n*-bit at nanoscale with low heat dissipation.

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Disclosure statement

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