A Novel Full Comparator Design Based on Quantum-Dot Cellular Automata

Davoud Bahrepour

***Abstract*—A lot of research has been done for implementing digital systems at nano-scale level. A quantum-dot cellular automaton (QCA) is a promising as well as emerging technology for implementing digital systems at nano-scale. QCA have attracted a lot of attention because of its extremely small feature size (at the molecular or even atomic scale) and its ultra-low power consumption, making it one candidate for replacing CMOS technology. This technology has been studied from a variety of physical and chemical aspects and in this paper, a novel full comparator design is introduced as a digital logic application for QCA-based circuits. Comparator is one of the important components in digital logic design and it widely used in central processing units (CPUs). The proposed design is compared with previous works in terms of area and delay. Comparisons show that the proposed design has improvement in area and delay.**

***Index Terms*—Full comparator, half comparator, quantum-dot cellular automata, nano-scale circuits.**

I. Introduction

CMOS technology has been a dominant technology for a long time and today scaling down of CMOS technology results in several limitations such as high leakage current, high power density levels, and high lithography cost [1]. To deal with these limitations, designers have employed new nanodevice technology such as QCA, single electron devices (SEDs), resonant tunneling diodes (RTDs), molecular electronics etc. as alternative solutions [2]-[10]. The QCA has become the very promising technology for designing the new generation of digital embedded systems. QCA has made the computations possible to be carried out at nano-scale. QCA is a transistorless computing paradigm that does not operate by the transport of electrons, but by the adjustment of electrons in a small limited area of only a few square nanometers. QCA offers notable advantages such as high density and high speed performance with low power consumption in the THz frequency [11]-[13]. Although QCA is still in its infancy, some experimental nanoelectronic devices have been manufactured with expected functionality [14]-[16].

II. QCA Basics

The main component of a QCA is a quantum cell that contains four quantum dot and two electrons. There are two diagonals in a QCA cell, which means the electrons can reside in exactly two possible adjustments in the cell. Regarding these two arrangements, they are interpreted as a binary '0' and binary '1'. These two distributions are encoded by logic 0 and logic 1, in which a P=-1 polarization equals 0 and a P=+1 polarization equals 1 in the binary format (Fig. 1). In other words, QCA is a binary logical architecture that encodes binary information by using its two polarizations [17].

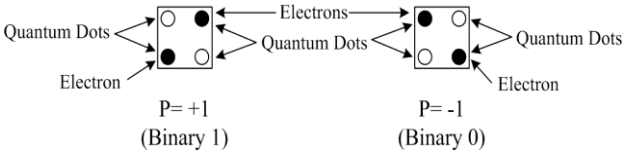

Fig. 1. QCA cell structure that generates logic 0 and logic 1.

QCA wire: A QCA wire consists of some QCA cells in a line. When two cells are close together, their electrons force each other and try to get minimum energy. The system energy would be minimized only when the cells states are the same. i.e., when the first cell has a specific arrangement (value), it copies its arrangement (value) to the neighbor cell and so on. Hence, the signal propagates through the line of cells and they work as a wire (Fig. 2). Two types of wires which are used in QCA technology are 90 º QCA wire and 45 º QCA wire. Fig. 2(a) shows a 90 ºQCA wire. This wire consists of a QCA array of cells in a line. A binary signal propagates from left to right because of electrostatic interactions between two neighbor cells [18], [19]. It is also possible to form a 45 º QCA wire (Fig. 2(b)). As shown in the figure a binary value propagates down the lengths of such wire, alternating between polarization P=+1 and polarization P=-1. This orientation among QCA cells represents the minimum energy configuration for each cell. As seen, there is both a complemented and uncomplemented signal value in 45 ºwire.

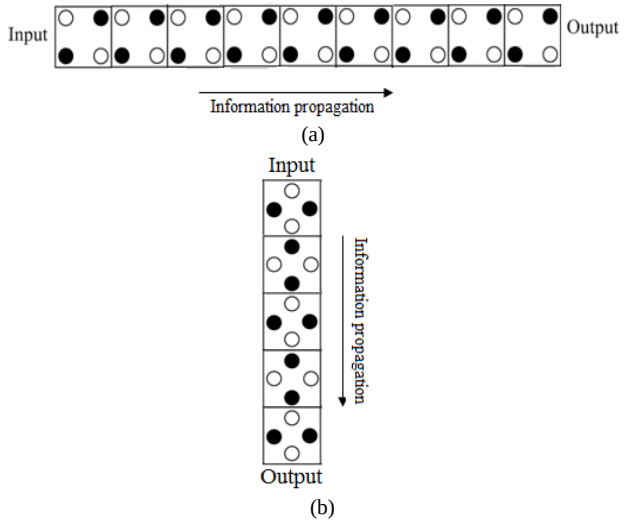

Fig. 2. Two types of QCA wire. (a) 90 ºQCA wire and (b) 45 ºQCA wire.

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QCA Clocking: As stated before the polarization of a QCA cell, switches between polarization P=+1 and polarization P=-1 when the two excess electrons tunnel between neighboring dots within the cell. When the interdot barrier is raised, a QCA cell will maintain its current polarization and will not react to the changes in the polarization of its neighbors. In order to control the interdot barrier of a QCA cell a clock is used (Fig. 3). This modulation of the interdot barrier in a QCA cell is a clock which controls data flow direction.

A QCA clock induces four stages in the tunneling barriers of the cells above it. These stages are: 1) switch; 2) hold; 3) release; and 4) relax [20]. During the switch phase, the interdot barrier starts to rise, and the QCA cell settles down to one of the two ground polarization states as influenced by its neighbors. During the hold phase, the interdot barrier is held high, preventing electron tunneling and maintaining the current ground polarization state of the QCA cell. During the release phase the interdot barrier starts to lower and during the relax phases, the interdot barrier allow electrons to freely tunnel again. In the last two phases, a QCA cell remains unpolarized. Overall, the polarization of a QCA cell is determined when it is in its switch phase by the polarizations of its neighbors that are in switch and hold phases.

Considering above statements, a clocked QCA design uses four clocks, namely: 1) Clock 1; 2) Clock 2; 3) Clock 3; and 4) Clock 4, Each clock is 90°out-of-phase from its previous clock.27 A group of QCA cells which are controlled by a same QCA clock form a QCA clocking zone. In QCA, four clocking zones are considered.

NOT Gate: Among QCA-based circuits one of the common gates is the NOT gate. As seen in Fig. 4, there are two types of NOT gates [18], [19]. In this gate, if the input equals logic 1, then the output will be logic 0 and vice versa.

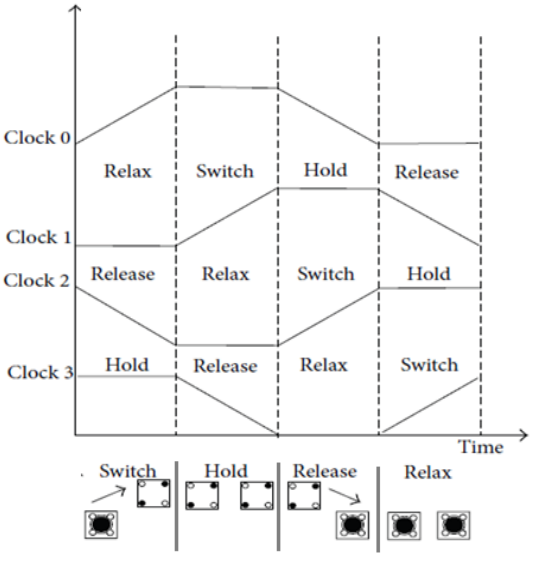


Fig. 3. The clock used in QCA.

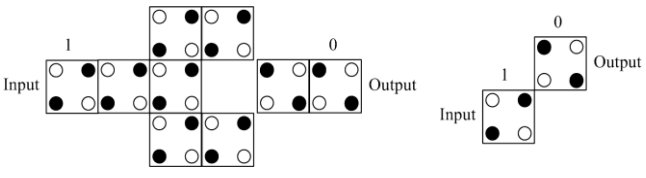


Fig. 4. Two types of the NOT gate.

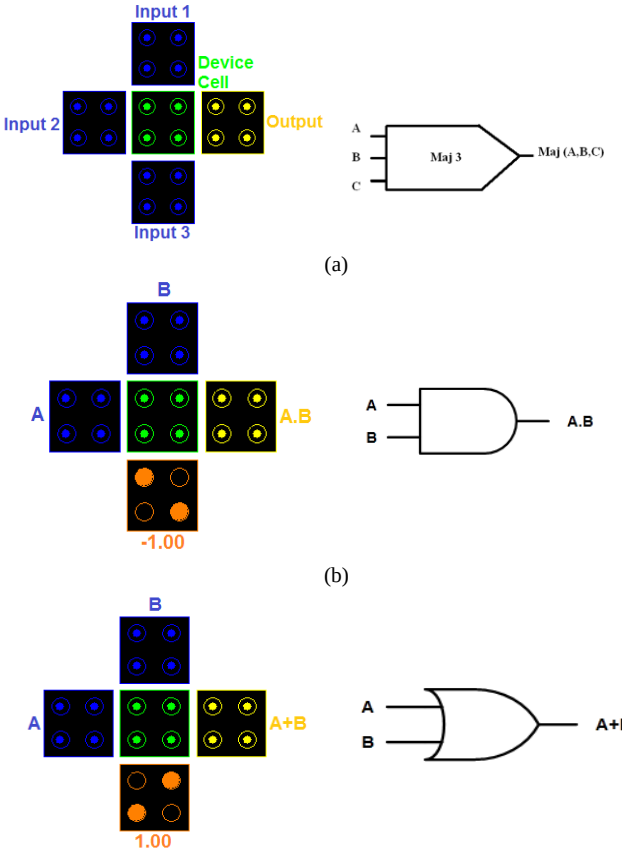


Fig. 5 (a) Three-input QCA majority funcyion at left and the logical symbol at right. (b) and (c) AND and OR gates based on three-input QCA majority funcyion.

Majority Gate: The most fundamental logical gate in QCA is the majority gate. The output of the majority function is logic 1 when the majority of inputs are logic 1, the output of a majority function is logic 0 when the majority of inputs are logic 0. To date, many QCA-based circuits have been designed based on the three-input majority function. As shown in Fig. 5(a) for implementing a majority function, three quantum cells as an input, one quantum cell as a device cell and one quantum cell for output are needed. The design of a QCA-based three-input majority function and its graphical symbol are illustrated in Fig. 5(a) and its Boolean function is represented in Eq.1. A logical equation for a majority gate is as:

$$Maj(A, B, C)=AB+AC+BC \quad (1)$$

Fig. 5(a) shows that the three-input majority function is implemented by five QCA cells. Achieving AND, OR gates based on three-input majority gate are shown in Fig. 5(b) and (c), respectively. Another common gate that has been designed in QCA is the five-input majority gate. The Boolean function of a five-input majority gate is presented in Eq. 2.

$$Maj(A,B,C,D,E)=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE \quad (2)$$

There are different types of five-input majority function in terms of cell counts and area [19], [21]-[24]. Hashemi et al. presented a five-input majority gate design with 17 cells (Fig. 6) [24]. The main feature of this design is that it accepts A, B,

C and D as inputs. In fact input D is used as two identical inputs in the gate. In other words, two inputs are connected to each other and named D.

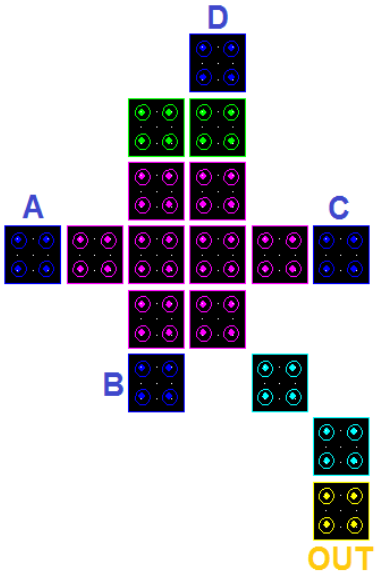


Fig. 6. Five-input majority function (input *D* acts as two inputs).

III. Designing a New Full Comparator

Comparison is the most basic arithmetic operation that determines if one number is greater than, equal to, or less than the other number. Comparator is the most fundamental component that performs comparison operation. The logical functions of the half comparator can be expressed as:

$$F_{A>B} = A\overline{B} \quad (3)$$

$$F_{A<B} = \overline{A}B \quad (4)$$

$$F_{A=B} = \overline{F_{A>B}}, \overline{F_{A<B}} \quad (5)$$

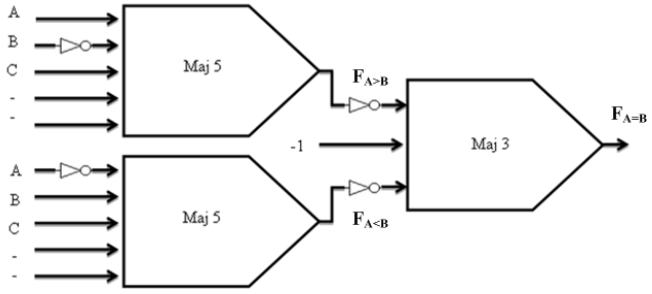
where A and B are inputs and $F_{A=B}$, $F_{A>B}$ and $F_{A<B}$ are the outputs. Considering Eq. 5 the full comparator is as:

$$F_{A>B} = A\overline{B}C \quad (6)$$

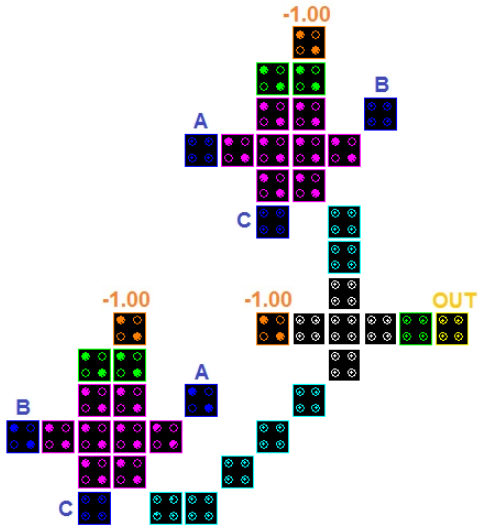
$$F_{A<B} = \overline{A}BC \quad (7)$$

$$F_{A=B} = \overline{F_{A>B}}, \overline{F_{A<B}} \quad (8)$$

where A and B are inputs and C is the comparison result of the previous stage and $F_{A=B}$, $F_{A>B}$ and $F_{A<B}$ are the outputs. It is clear that by adjusting the input C equal to 1 the full comparator acts as a half comparator. A full comparator realized with majority gates and inverters is illustrated in Fig. 7(a). The novel design of the full comparator based on QCA is shown in Fig. 7(b). As seen in Fig. 7(b), the design utilizes two five-input majority functions and one three-input majority function. This circuit generates the $F_{A>B}$ and $F_{A<B}$ at the same time and the $F_{A=B}$, 0.25 clock cycles later. To verify the correct operation of the proposed circuit, QCA Designer tool ver.2.0.2 is utilized [25].



(a)



(b)

Fig. 7(a) Gate level design for a full comparator. (b) The novel full comparator design based on five-input majority function.

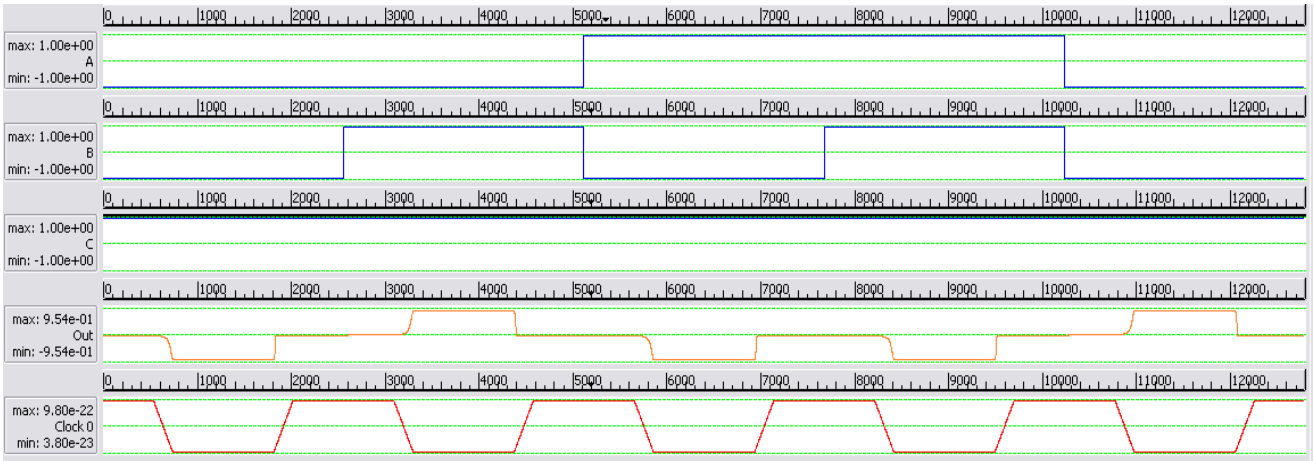


Fig. 8. The proposed full comparator simulation result. The first three waveforms are the inputs and the fourth one is the output. The last waveform is clock 0 which generates the output.

TABLE I: THE FULL COMPARATOR CIRCUIT PARAMETERS

Number of samples	12800	*clock low*	3.800000e-23
convergence tolerance	0.001000	*cell distance [nm]*	2
radius of effect [nm]	65.000000	*clock amplitude factor*	2.000000
relative permittivity	12.900000	*layer separation*	11.500000
clock high	9.800000e-22	*maximum iterations per sample*	100
cell size [nm]	18 ×18	*the diameter of the quantum dot [nm]*	5

TABLE II: COMPARISON OF QCA COMPARATORS

QCA Full Comparator	*# of levels*	*Complexity (cells)*	*Area [μm^2]*	*Time delay (clock cycle)*
Full Comparator (2008) [24]	3	* ULG based design = 363	Not reported	ULG based design= 2.25
		* MI based design = 166		MI based design= 1.5
Full Comparator (2014) [25]	2	48	Not reported	1.25
The proposed Full Comparator	2	43	0.08	1.25

* After removing the unnecessary cells

IV. SIMULATION RESULTS AND COMPARISONS

The applied input signals and resulting output waveform are depicted in Fig. 8. The first three waveforms represent the input signals (A, B and C) and the fourth waveform represents the output signal ($F_{A=B}$). The first meaningful output appears in second clock tick after 1 clock delay. It can be seen that the full comparator has correct logic function.

During simulation, the simulation engine, bistable approximation, is chosen and the adjusted values are shown in Table I. Table II shows the comparison between the proposed full comparator and the previous ones. As shown in Table II, the new design has resulted in significant improvements in terms of area and time delay in comparison with [26]. Also the proposed full comparator has 5 cells less than [27].

V. CONCLUSION

In this paper, a novel QCA full comparator design was proposed. Full comparators are widely used in central processing units (CPUs) and any improvement in full comparator design leads to achieving high performance CPUs. For investigating the correct operation of the full comparator circuit the QCA Designer tool is used. The proposed design shows improvement in terms of cell counts, and time delay. In comparison with the best previous full comparator, the proposed design achieves 10% reduction in terms of number of cell counts. Since its time delay is 1.25 clock cycles, therefore, it is considered as a high speed full comparator.

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