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Design of Low-Power Low-Area Tunable Active RC filters

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***Abstract*—A method to design low-power low-area active RC filters is presented. The output voltages of the operational amplifiers (opamps) are scaled and buffered allowing the use of single stage topologies for less power consumption and eliminating the compensation capacitor. Tuning of the filter characteristic is also done by switching the currents through the output buffers which removes the need for capacitor banks. The advantages of the proposed method are incorporated to present a general low-power biquad with small die area. The biquad section is then used to design a low power baseband filter for Bluetooth receivers with 600 KHz cutoff frequency. The fourth-order filter, fabricated in a 0.18 μm CMOS process, consumes 0.5 mW with a die area of 0.13 mm^2.**

***Index Terms*—Active RC filter, Low power, Low area, Tunable, Bluetooth**

I. Introduction

Demand for higher performance and more functionality for hand-held systems have been continually growing in the recent years. Improved performance and more functionality, however, often come with more power consumption. This is why new low power design techniques and circuits have become one of the major subjects of research and innovation. Active RC filters as a part of many systems that are integrated on the chip are no exception. That is they must be low power and the area that they occupy on the silicon chip must be as small as possible.

Active RC filters have superior linearity compared to other techniques such as Gm-C filters due to the closed loop nature of integrators [1]. In conventional active RC filters, operational amplifiers (opamps) are used as integrators, thus, power consumption of the filters are directly related to that of opamps. Because of the resistor or capacitor variation in the fabrication process, tuning is also inevitable and using capacitor banks for the tuning considerably increases the die area [2].

Novel methods with a variety of techniques for reducing circuit power consumption and increasing the design performance have been reported. For example: the elaborate method in [1] using a replica circuit for tuning; anti-pole-splitting technique [3] which enhances the gain-bandwidth (GBW) of the opamp without extra power consumption; or the work in [4] that uses low-power low gain opamps by compromising the linearity and precision of the filter for less power consumption.

In this paper, we propose a method with reduced power consumption, easy tuning and small die area. The output stage in conventional two-stage Miller compensated opamps consumes considerable power for driving capability. To save silicon area and power consumption, the opamps used in the proposed method are single-stage, hence eliminating the need for the large compensation capacitors. Tuning is also done without using capacitor banks, which helps to further reduce the die area.

Using the proposed method, design of a low power fourth-order Butterworth low pass filter for the zero-IF Bluetooth receiver is explained and the measurement results of the fabricated chip are presented.

The basic idea is described in section II, in section III a low-noise biquad section based on the proposed method is presented. Section IV is devoted to circuit implementation of the filter including tuning and the design of the low-power opamps. In section V, a fourth-order low-pass filter suitable for Bluetooth receivers is presented. Section VI presents the measurement results of the fabricated chip and finally the conclusions are drawn in section VII.

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II. Basic Idea

Let's consider the lossy integrator in Fig. 1(a). Assuming that the low-frequency gain of the opamp is large enough, the voltage transfer function of the circuit can be written as

$$\frac{V_o}{V_{in}} = -\frac{\frac{R_1}{R_{in}}}{R_1 C_1 s + 1} \tag{1}$$

Let's now consider the integrator in Fig. 1(b) where a gain stage of $\frac{1}{n}$ is interposed between the output of the opamp and the feedback resistor ${R_1}'$. The transfer function of the modified integrator can be derived as

$$\frac{V_o}{V_{in}} = -\frac{\frac{n{R_1}'}{R_{in}}}{n{R_1}' C_1 s + 1} \tag{2}$$

Comparison of (2) with (1) directly shows that if the resistor ${R_1}'$ in Fig. 1(b) is

$${R_1}' = \frac{R_1}{n} \tag{3}$$

then the circuit in Fig. 1(b) will have the same transfer function as that of the conventional integrator in Fig. 1(a). The advantages of the modified integrator in Fig. 1(b) over the original integrator may be summarized as

- Pole location can be tuned by adjusting n thus eliminating the need for the capacitor bank.
- Since ${R_1}'$ is isolated from the output node of the opamp, single-stage opamps can be used hence avoiding the need for the compensation capacitor.
- Lower power consumption by the opamps due to elimination of the output stage of the opamps.

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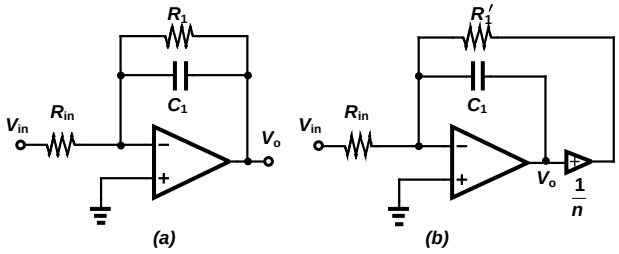

Fig. 1. (a) Lossy integrator (b) integrator with $\frac{1}{n}$ at the output.

III. Low Power low Noise Biquad Section

A Tow-Thomas [5] biquad is shown in Fig. 2(a) whose transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_{in}R_2C_1C_2}}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4}$$

where,

$$\omega_0 = \frac{1}{\sqrt{R_2R_3C_1C_2}} \tag{5}$$

and

$$Q = \sqrt{\frac{{R_1}^2C_1}{R_2R_3C_2}} \tag{6}$$

Let's assume the output voltage of the opamps are first divided by $n_i > 1$ and are then applied to the resistors at the output. This is shown in Fig. 2(b) from which the transfer function of the new circuit can be derived as

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_{in}R_2{}'n_1C_1C_2}}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{7}$$

where,

$$\omega_0 = \frac{1}{\sqrt{n_1n_2R_2{}'R_3{}'C_1C_2}} \tag{8}$$

and

$$Q = \sqrt{\frac{n_1{R'}_1{}^2C_1}{n_2{R'}_2R'_3C_2}} \tag{9}$$

By comparing Equations (7) to (9) with those in (4) to (6) we can conclude that for the transfer function of the modified circuit remains the same, resistors ${R_1}'$ to ${R_3}'$ are to be the same as R_1 to R_3 but divided by n_i.

The equivalent input noise voltage of the modified Tow-Thomas biquad in Fig. 2(b) can be calculated as in (10) that is shown at the bottom of this page where, $\overline{{V_{n_{in-op1}}}^2}$ and $\overline{{V_{n_{in-op2}}}^2}$ are the equivalent input noise voltages of the first and the second opamp, respectively. As it can be seen from

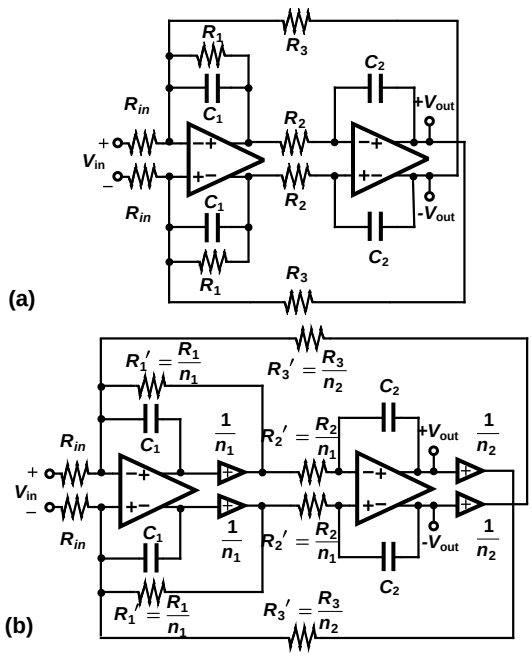

Fig. 2. (a) Tow-Thomas biquad (b) Modified Tow-Thomas biquad circuit.

(10), the noise voltage due to R_{in} remains unchanged while that of R_1, R_2 and R_3 are increased by a factor of $\sqrt{n_i}$.

In practical cases where the voltage gain of the first stage is large enough (to reduce the effect of the second stage's noise) and the dominant part of the noise is due to the opamps, equation (10) in the pass-band frequencies of the filter (low frequencies) can be approximated as

$$\overline{{V_{n_{in}}}^2} \approx \left[1 + \frac{R_{in}}{{R_1}'} + \frac{R_{in}}{{R_3}'}\right]^2 \overline{{V_{n_{in-op1}}}^2} \tag{11}$$

To compensate for the higher equivalent noise voltage at the input, the method presented in [6] is used to improve the noise behavior of the biquad section. As shown in Fig. 3(a), this is done by inserting a feed-forward amplifier in the circuit. The feed-forward amplifier measures the noise at the input of the first opamp in the biquad section and feeds it to the input of the second opamp. Note that, as explained in [6], the feed-forward opamp does not disturb or change the circuit transfer function of the desired signal and it is only the noise at the input of the first opamp that is sampled and fed forward. The gain of the feed-forward opamp for the optimum circuit noise performance [6] can be approximated as

$$A_f = 1 + \frac{{R_1}'}{R_{in}} + \frac{{R_1}'}{{R_3}'} \tag{12}$$

$$\overline{{V_{n_{in}}}^2} = 4KT\left[\underbrace{R_{in}}_{R_{in}} + \underbrace{\frac{{R_{in}}^2}{{R_1}'}}_{R'_1} + \underbrace{\left(\frac{R_{in}}{{R_1}'}\right)^2\left(1 + {R_1}'C_1s\right)^2{R_2}'}_{R'_2} + \underbrace{\frac{{R_{in}}^2}{{R_3}'}}_{R'_3}\right] + \tag{10}$$
$$\left[1 + \frac{R_{in}}{{R_1}'} + \frac{R_{in}}{{R_3}'} + R_{in}C_1s\right]^2\overline{{V_{n_{in-op1}}}^2} + \left[\frac{R_{in}}{{R_1}'}\left(1 + {R_1}'C_1s\right)\left(1 + {R_2}'C_2s\right)\right]^2\overline{{V_{n_{in-op2}}}^2}$$

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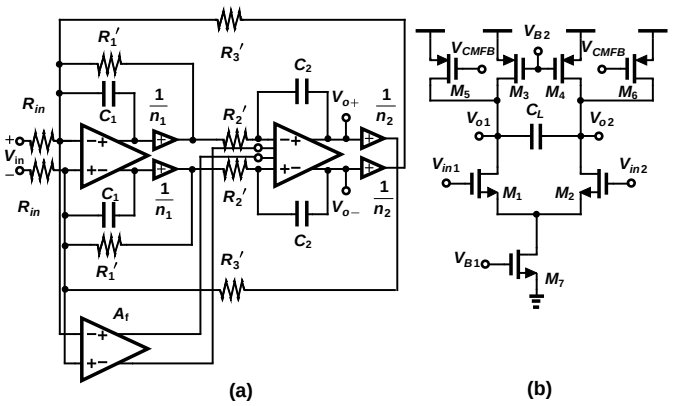

Fig. 3. (a) Biquad with the feedforward amplifier for noise cancellation (b) Feedforward amplifier (common mode feedback is not shown.)

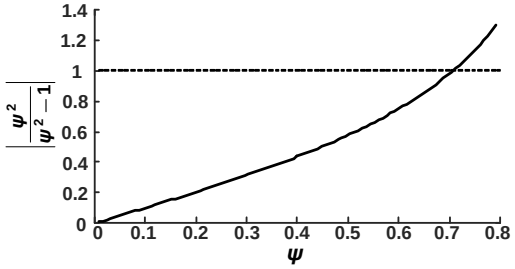

Fig. 4. Noise improvement factor as a function of ψ.

The equivalent input noise voltage of the biquad section of Fig.3(a) can then be calculated [6] as

$$\overline{V_{n_{in}}{}^2} \approx \left[1 + \frac{R_{in}}{R_1{}'} + \frac{R_{in}}{R_3{}'}\right]^2 \overline{V_{n_{in-op1}}{}^2} \times \left|\frac{\psi^2}{\psi^2 - 1}\right| \quad (13)$$

Where, $\psi^2 = \frac{\overline{V_{n_{in-Af}}{}^2}}{\overline{V_{n_{in-op1}}{}^2}}$ and $V_{n_{in-op1}}$ and $V_{n_{in-Af}}$ are the equivalent input noise voltage of the first opamp and the feed-forward amplifier, respectively. Equation (13) shows that the feed-forward amplifier improves the noise behavior of the circuit by a factor of $|\frac{\psi^2}{\psi^2-1}|$. Fig. 4 shows the improvement factor $|\frac{\psi^2}{\psi^2-1}|$ as a function of ψ. As it can be seen from Fig. 4, for $\psi = .7$ the improvement factor is 1 and the feed-forward amplifier has no effect on the circuit performance. As ψ is made smaller, that is the feed-forward amplifier injects less noise in the circuit, the improvement factor and consequently the overall circuit noise become smaller. This is why the feed-forward amplifier is designed as a simple low noise differential stage as shown in Fig. 3(b).

IV. Circuit implementation

To implement the $\frac{1}{n_i}$ stage in Fig. 3(a), a source follower stage is interposed between the feedback resistor of the lossy integrator and the opamp's output, as shown in Fig. 5(a). Assuming the low-frequency gain of the opamp is large enough, the transfer function of the modified integrator, $\frac{V_o}{V_{in}}$, is as given in (2) in which n_i is defined as

$$n_i = 1 + \frac{1}{g_{m_{Buffer}} R_1{}'} \quad (14)$$

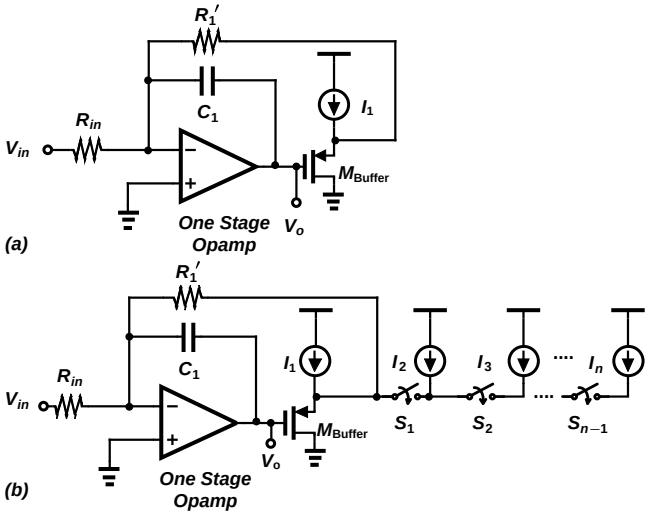

Fig. 5. (a) Source follower as $\frac{1}{n}$ stage. (b) Tuning method for the integrator.

where, $g_{m_{Buffer}}$ is the transconductance of M_{Buffer}.

A. Tuning

As it can be seen from (2), the integrator's pole is dependent on n_i, that can be adjusted by adjusting the bias current of the source follower buffer. The current sources and the switches in Fig. 5(b) provide the facility to fine tune n_i and the pole of the lossy integrator. This removes the need for R-ladder or C-ladder that are conventionally used for tuning active RC filters.

B. Low Power Opamp

A single-stage opamp as opposed to multi-stage is used to avoid the need for compensation capacitor and to save the second stage power consumption. This is made possible because the load resistors are not directly connected to the opamps output, hence eliminating the need for a driver stage. A folded cascode gain stage, as shown in Fig. 6 is used to realize the opamps of the biquad section. As it can be seen in Fig. 6, the differential pair M_3 and M_4 create a signal path through the current mirrors M_5, M_7 and M_6, M_8 and increase the opamp transconductance by a factor of k [7] resulting in a higher GBW for the opamp. That is the transconductance of the folded cascode stage becomes

$$G_m = g_{m1} + \frac{k g_{m3}}{g_{m7}} . g_{m5} \quad (15)$$

Though a large value of k improves opamp's GBW, it also lowers the 2nd pole at the mirror node causing smaller phase margin and possible instability. To alleviate the problem, the second pole of the opamp at the mirror nodes is nulled and pushed to higher frequencies by a negative capacitance circuit as shown in Fig. 6.

For the second pole moves to higher frequencies by a factor of x the output resistance of the current sources $M_{16,17}$ must be much larger than $\frac{1}{g_{m7,8}}$ and C_N is to be chosen such that

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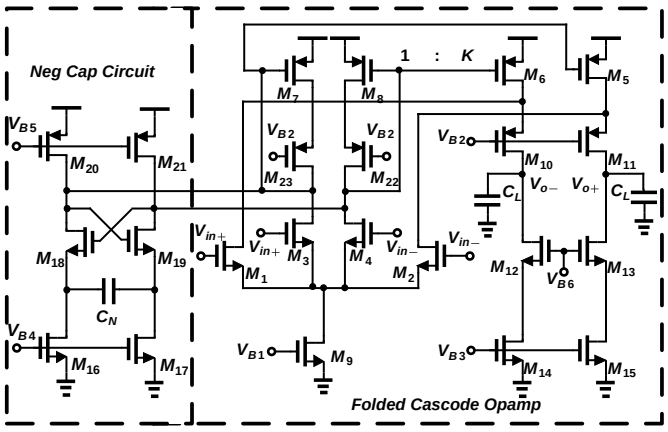

Fig. 6. Single-stage opamp with negative capacitance circuit for BW enhancement.

TABLE I
SIMULATION RESULTS OF THE OPAMP IN FIG.6.

DC gain	Gain-Bandwidth	Phase margin	Power	C_L	Slew rate
70 dB	24 MHz	60°	81 μW	2 pF	40 $V/\mu S$

TABLE II
MEASURED PERFORMANCE AND COMPARISON WITH STATE-OF-THE-ART.

Specification	[9]	[3]	[1]	[10]	This work
Technique	Gm-C	Active RC	Active RC	Active RC + DT	Active RC
Technology (μm)	0.18	0.12	0.13	0.065	0.18
Order	3	5	5	4	4
Bandwidth (MHz)	0.5	5	19.7	10	0.6
DC Gain (dB)	0	0	2	0	10
Input noise $nV/\sqrt{Hz}$	425	140	30	22.8	126
IIP3 (dBm)	22.3	20	18.3	11	25
SFDR (dB)	57.3	73	69	58	65.6
Power (mW) @ VDD	4.1 @1.2	6.1 @1	11.25 @1.5	10.8 @1.8	0.5 @1.8
Chip Area (mm^2)	0.23	0.25	0.2	0.75	0.14
FOM ($fJ.\mu m^2$)	6900	30.5	42.6	25493	25.4

$FOM = \frac{Power \times Area}{Order \times SFDR \times Bandwidth \times IIP3}$ [3]

[8]

$$C_N \approx \left(1 - \frac{\sqrt{2}}{x}\right) C_p \tag{16}$$

where, C_p is the total parasitic capacitance at the gate of $M_{5,6}$. The transconductance of the negative capacitance circuit, $g_{m_{18,19}}$, must also be chosen such that [8]

$$g_{m_{18,19}} = \left(x^2 - x\sqrt{2}\right) g_{m_{7,8}} \tag{17}$$

The simulation results of the opamp designed in a 0.18μm CMOS process are given in Table I.

V. FOURTH-ORDER BASE-BAND FILTER

Two main design requirements for the frequency characteristic of the base-band filter in the zero IF Bluetooth application are f_{-3dB} = 600 KHz and 30 dB Adjacent channel rejection at 2 MHz offset from the center frequency of the receiver.

To satisfy the requirements, a fourth-order Butterworth transfer function with the pass-band gain of 10 dB and 42 dB attenuation at the frequency of the adjacent channel has been chosen. Two biquad sections were used to realize the transfer function. The first biquad section includes the noise cancelling feed-forward path that is shown in Fig. 7(a).

VI. MEASUREMENTS

The filter of Fig. 7(a) was fabricated in a 0.18 μm CMOS technology with a die area of 0.13 mm^2. The microphotograph of the chip is shown in Fig. 7(b).

The Q and ω_0 of the filter can be directly tuned to desired values by changing n_i (1.1< n_i <4). For each buffer, 6 bits are used for tuning. As can be seen from (9), Q is a function of the ratios of resistors and capacitors that makes it fairly insensitive to the process variations though it can be changed by changing either n_1 or n_2. The frequency ω_0, as shown by (8), varies with the process variations and needs adjustments by changing either n_1, n_2 or both. It is interesting to note that, for tuning ω_0 , if n_1 and n_2 are changed simultaneously while maintaining the ratio $\frac{n_1}{n_2}$, the filter's quality factor (Q) remains constant. Fig. 8(a) shows the measured frequency characteristics of the filter where the cutoff frequency of the filter is changed from 300 KHz to 1 MHz by simultaneously changing n_1 and n_2 for the constant Q.

The filter output voltage for a 1 KHz, 60 mV sinusoidal input voltage is shown in Fig. 8(b). The linearity of the filter was evaluated by measuring IIP3 of the filter. As it is shown in Fig. 9(a), the filter's IIP3 is at 25 dBm. Measured equivalent noise voltage of the filter is shown in Fig. 9(b).

Table II presents a comparison of this work with some of the recently published results.

VII. CONCLUSION

In this paper a new method to design low-power filters is presented. We have shown that by isolating the resistive load from the integrator's opamp output the design of the low-power opamp for the integrator can be greatly facilitated. It was also shown that the isolation can be simply done by inserting a source follower buffer at the output. The voltage transfer gain of the buffer can be set at the desired value by adjusting the DC current through the buffer. The frequency response of the filter can then be directly controlled by adjusting the current through the output buffers. It was shown that by the proposed technique low-power tunable biquad and therefore high-order filters with FOM better than previously reported methods can be designed.

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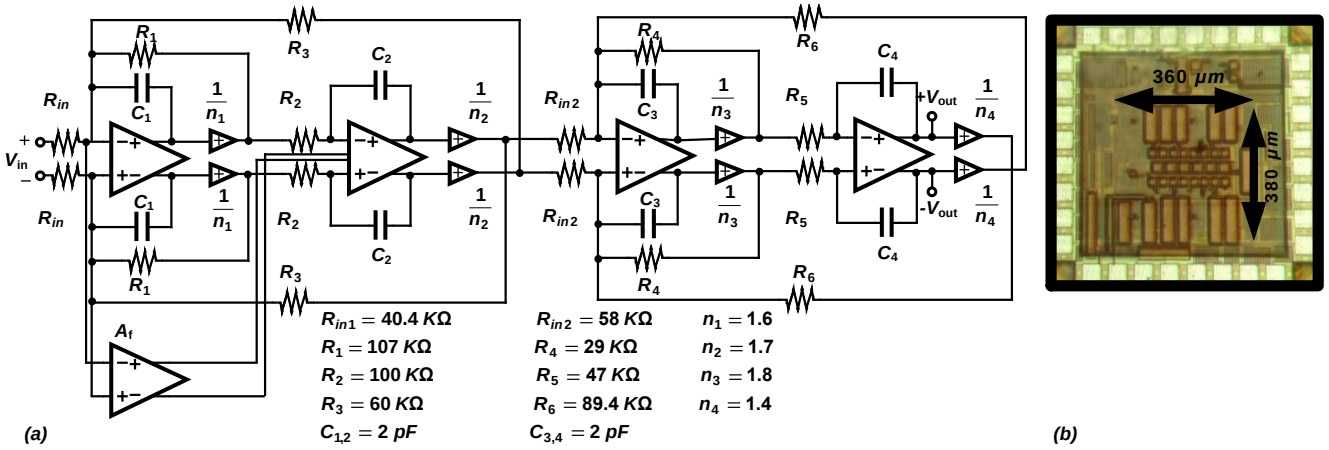

Fig. 7. (a) Fourth-order filter for Bluethooth application. (b) Microphotograph of the Bluetooth filter.

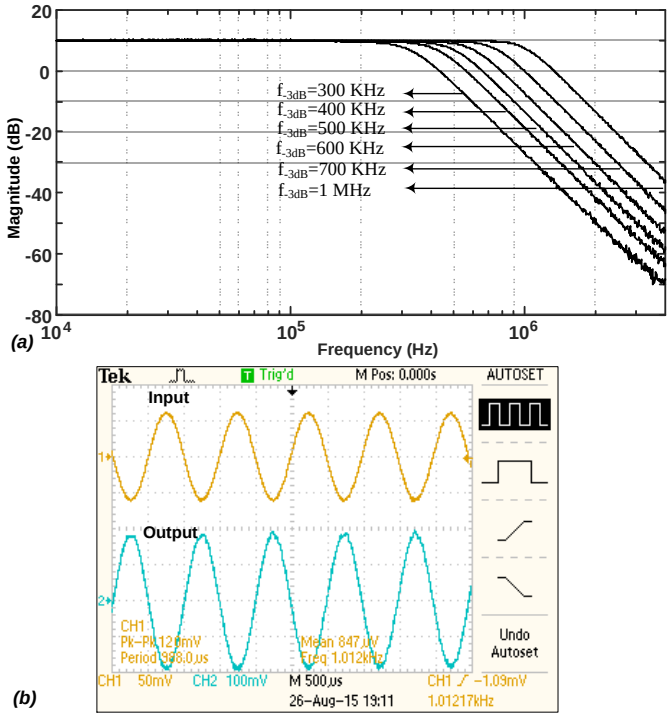

Fig. 8. (a)Frequency response of the filter. (b) Filter's output waveform for a 1KHz, 60mV sinusoidal input voltage.

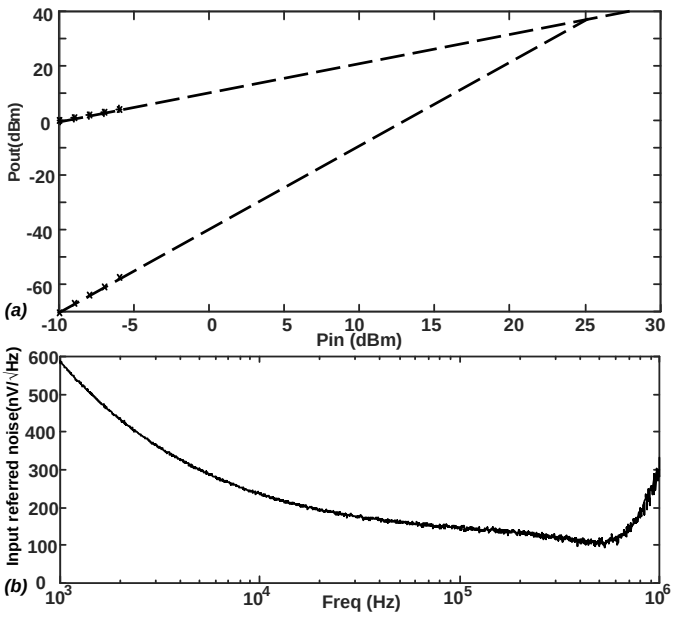

Fig. 9. (a) Measured IIP3 of the filter. (b) Measured input equivalent noise voltage.

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