Design and Optimization of Full Comparator Based on Quantum-Dot Cellular Automata

Mohsen Hayati and Abbas Rezaei

Quantum-dot cellular automata (QCA) is one of the few alternative computing platforms that has the potential to be a promising technology because of higher speed, smaller size, and lower power consumption in comparison with CMOS technology. This letter proposes an optimized full comparator for implementation in QCA. The proposed design is compared with previous works in terms of complexity, area, and delay. In comparison with the best previous full comparator, our design has 64% and 85% improvement in cell count and area, respectively. Also, it is implemented with only one clock cycle. The obtained results show that our full comparator is more efficient in terms of cell count, complexity, area, and delay compared to the previous designs. Therefore, this structure can be simply used in designing QCA-based circuits.

Keywords: Quantum-dot cellular automata, QCA cell, QCADesigner, majority gate, full comparator.

I. Introduction

In the last few decades, scaling the feature size and increasing the processing power have been successfully achieved by conventional lithography based on VLSI technology [1]. However, it seems that even by decreasing the transistor sizes, some problems such as high power consumption and difficulties in feature size reduction cannot be ignored. Research predicts that CMOS technology may hit physical scaling limits in 2012 and will be superseded by some emerging technologies. Nanotechnology is an alternative to these problems, and the ITRS report [2] summarizes several possible technology solutions. Relying on the unique properties of electronic devices at nanoscale feature size, nanotechnology opens up new horizons for computing systems and devices. Quantum-dot cellular automata (QCA) is an emerging technology that offers a revolutionary approach to computing at nano-level. QCA proposed by Lent and others [3] created general computational functionality at the nanoscale by controlling the position of a single electron. This technology promises extra low power, high speed, and extremely dense circuits. Using QCA technology for the implementation of logic circuits not only increases the clock frequency of logic circuits and decreases the size of these circuits, but also reduces the power consumption of these circuits [4]. Furthermore, the circuits based on the QCA have the ability of highly parallel processing [5]. One of the basic digital devices, and probably a vital part of many modern computing platforms, is the comparator. Previously, comparator designs were examined for implementation with QCA technology [6]-[10]. In this letter, we propose an optimized full comparator based on QCA implementation working with only 4 clock phases. This design requires a minimum number of cells and area allocations as compared to the previous works [6]-[10].

II. QCA Basis

The fundamental unit of QCA is the QCA cell, which is composed of four quantum dots, as shown in Fig. 1(a) [11], [12]. The cell is charged with two extra electrons, which tend to occupy diagonally opposed dots as a result of their coulomb repulsion. The electrons are permitted to jump between the various quantum dots in a cell by the mechanism of quantum mechanical tunneling, but they are not permitted to tunnel between the two individual cells [12]. Thus, there are two possible arrangements denoted as cell polarization P=+1 and P=–1. By using cell polarization P=+1 to represent logic 1 and

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P=–1 to represent logic 0, binary information can be encoded. Arrays of QCA cells can be arranged to perform wire and all logic functions [11]. Instead of the traditional metal wire, the QCA wire is used to construct a digital logic circuit. In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between the cells. There are two kinds of QCA wires as shown in Fig. 1(b) and Fig. 1(c). One is a binary wire implemented with the cells of 90º orientation, and the other is an inversion chain implemented with the cells of 45º orientation. Each cell in the inversion chain takes on the opposite polarization of its neighbors [12]. Fig. 1(d) shows the QCA multilayer crossing structure. Multilayer crossing is constructed by adding more layers [13]. Any QCA circuit can be efficiently built using only majority gates and inverters. The simplest structure of the inverter, shown in Fig. 1(e), is usually formed by placing the cells only with their corners touching. In Fig. 1(f), the 45º displacement in the two lines of merging cells produces the complement of the input signal [11]. Figure 1(g) shows the gate symbol of the inverter. The fundamental logic gate for QCA is the 3-input majority gate composed of 5 cells. Figures 1(h) and 1(i) show the QCA layout and its gate symbol, respectively. Assuming that the inputs are *a*, *b*, and *c*, the logic function of 3-input majority gate can be expressed as [12]

$$f = a.b + b.c + a.c = M(a, b, c). \tag{1}$$

The logic AND and logic OR functions can be implemented by a majority gate by setting one of their inputs permanently to 0 and 1, respectively. Inverters and majority gates provide a functionally complete logic set for QCA. Various QCA circuits, including combinational as well as sequential circuits have been proposed in [4]-[12].

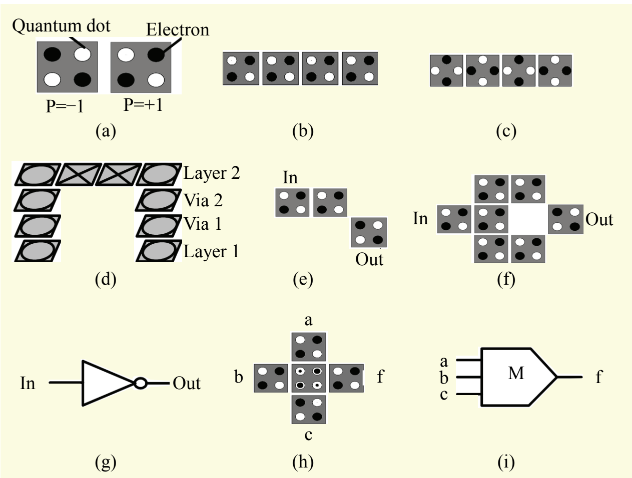

Fig. 1. (a) QCA cell, (b) binary wire, (c) QCA inversion chain, (d) QCA multilayer crossing, (e) QCA inverter type 1, (f) QCA inverter type 2, (g) circuit diagram of inverter, (h) QCA implementation of majority gate, and (i) circuit diagram of majority gate.

III. Design Approach

Comparator is one of the important components in logic design. Comparators are used in central processing units (CPUs) and microcontrollers. If we assume that the inputs are A and B and the outputs are $O_{A=B}$, $O_{A>B}$, and $O_{A<B}$, the logical functions of the half comparator can be expressed as

$$\begin{aligned} O_{A>B} &= A.\overline{B}, \\ O_{A<B} &= \overline{A}.B, \\ O_{A=B} &= \overline{O}_{A>B}.\overline{O}_{A<B}. \end{aligned} \tag{2}$$

Also, the equations for a full comparator are given by

$$\begin{aligned} O_{A>B} &= A.\overline{B}.C, \\ O_{A<B} &= \overline{A}.B.C, \\ O_{A=B} &= \overline{O}_{A>B}.\overline{O}_{A<B}, \end{aligned} \tag{3}$$

where for an *n*-bit full comparator, the output $O_{A=B}$ of one stage is fed directly to the input C of the next stage. The logic diagram of a full comparator is presented in Fig. 2(a). Equations for a full comparator realized with majority gates and inverters are shown below:

$$\begin{aligned} O_{A>B} &= M(M(A, \overline{B}, -1), -1, C), \\ O_{A<B} &= M(M(\overline{A}, B, -1), -1, C), \\ O_{A=B} &= M(\overline{O}_{A>B}, \overline{O}_{A<B}, -1). \end{aligned} \tag{4}$$

Figure 2(b) shows the schematic diagram of the full comparator based on majority gates and inverters, and Fig. 2(c) shows the proposed QCA layout of the full comparator.

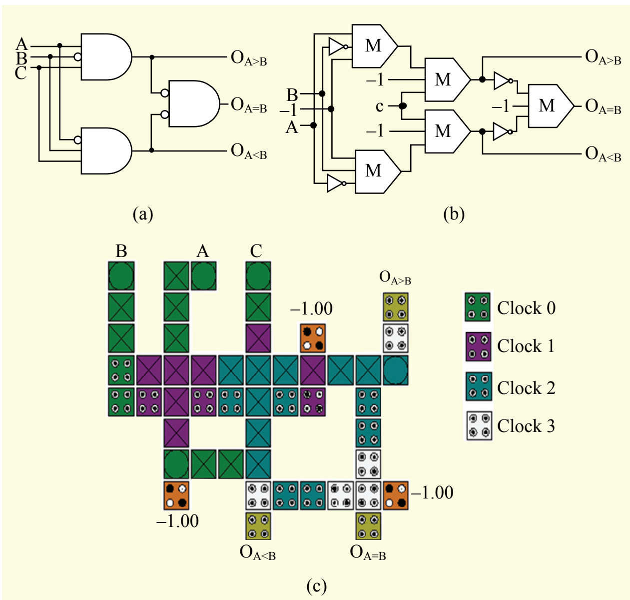

Fig. 2. QCA full comparator: (a) logic diagram, (b) implementation with majority gates and inverters, and (c) proposed QCA layout.

IV. Results and Discussion

The QCA implementation of the proposed full comparator is simulated by the QCADesigner tool [14]. The following parameters are used for a bistable approximation [14]: cell size=18 nm×18 nm, number of samples=12,800, radius of effect=65 nm, relative permittivity=12.9, convergence tolerance=0.0001, clock high=9.8e–22J, clock low=3.8e–23J, clock amplitude factor=2, layer separation=11.5 nm, and maximum iterations per sample=100. Also, the diameter of the quantum dot is 5 nm and the cell distance is 2 nm. The input and output waveforms for the proposed full comparator are shown in Fig. 3. Table 1 shows the comparison between the proposed full comparator and the previous ones, where HC, FC, and SC stand for half comparator, full comparator, and serial comparator, respectively. As shown in Table 1, our full comparator has resulted in significant improvements in terms of area, complexity, and delay. In comparison with the best previous full comparator design presented in [6], the proposed full comparator has 85% improvement in the area, 64% improvement in cell count, and 95% improvement in the wasted area in the cells. In comparison with the best previous half comparator presented in [9], our design has 62% improvement in the area, 16% improvement in the cell count, and 90% improvement in the wasted area in cells. Also, our comparator is faster than the previous ones. From these results, it is evident that the proposed full comparator is improved as compared to the previous ones.

In comparison to the previous works that have used coplanar crossing, we used a two-layer layout in our design. We have designed the logical structures using a 2-cell inverter instead of a 7-cell inverter. By applying this method, the hardware requirements for a QCA design can be reduced. Also, we have done part of the calculation in layer two to obtain the outputs that make the proposed layout an efficient design with a minimum number of cells, smaller size, and less delay. These methods can be applied to other QCA circuits, such as Full Adder, to reduce the hardware requirements for a QCA design.

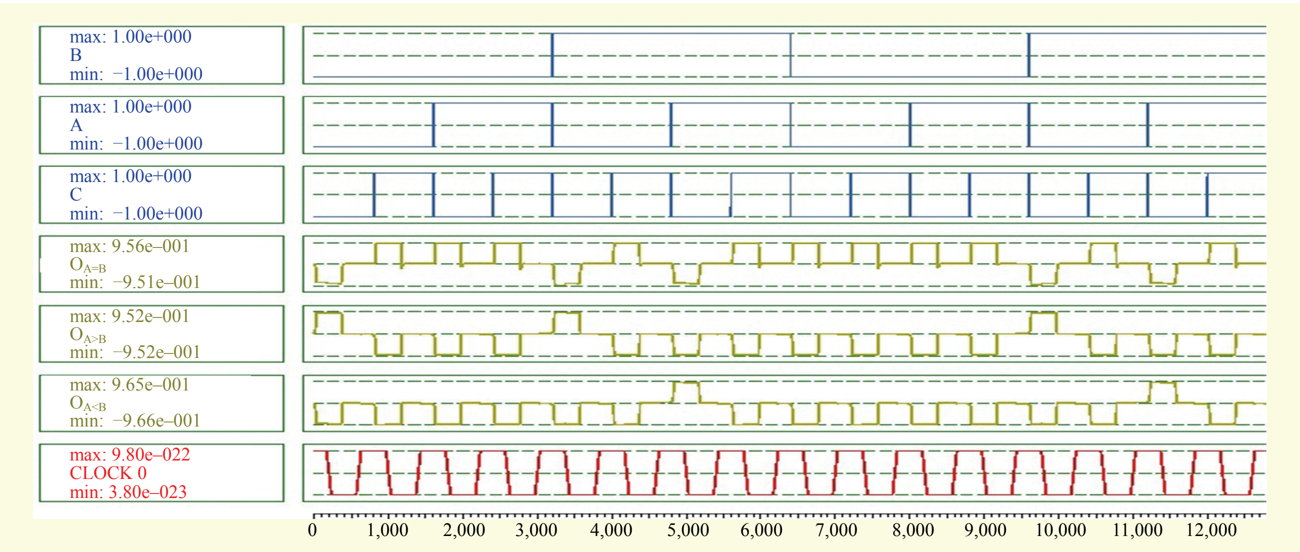

Fig. 3. Simulation results for proposed full comparator.

Table 1. Comparison of QCA comparators.

Reference	Type	Type of crossing	Cell count	Approximated area (μm^2)	Approximated wasted area in cells	Time delay (clock phase)
[6]	FC	Coplanar	222	0.262	468	8
[7]	HC	Coplanar	100	0.127	230	5
[8]	SC	Coplanar	221	0.338	670	9
[9]	HC	Coplanar	95	0.103	209	5
[10]	FC	Coplanar	262	-	-	9
Proposed design	FC	Two-layer	79	0.0388	20	4

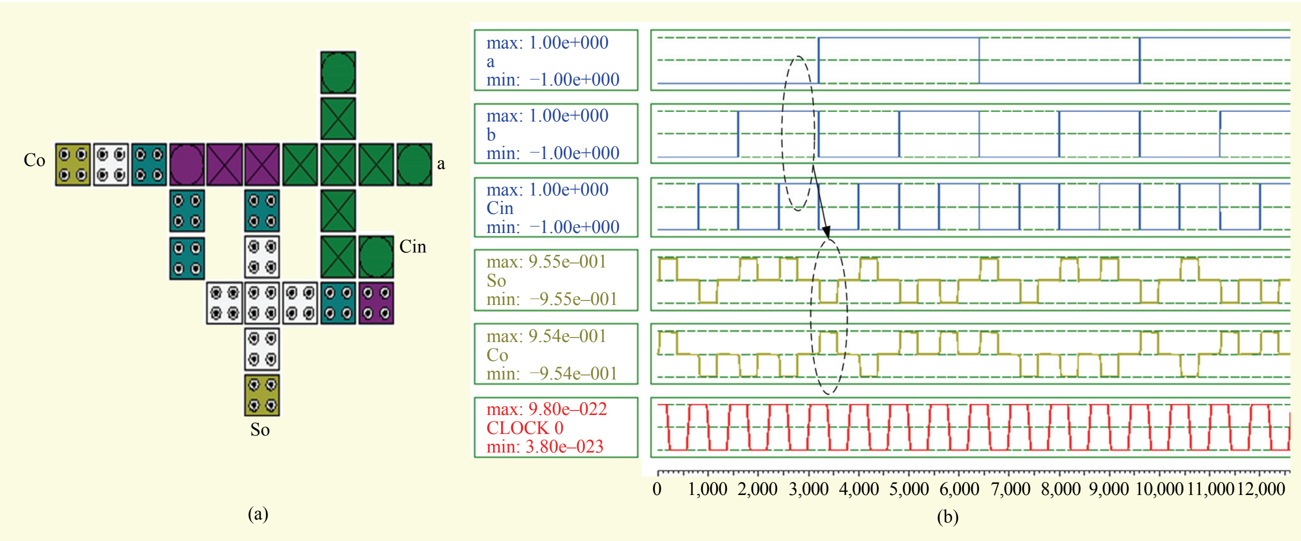

Fig. 4. One bit Full Adder: (a) layout and (b) simulation results.

Figure 4(a) shows a one-bit Full Adder implemented using these methods with only a 44 cell count, 4-clock phase delay, and an area of approximately 0.031 μm^2. The simulation result for this Full Adder is shown in Fig. 4(b). The proposed Full Adder is compared with a previous work presented in [13], which has a 101 cell count, 8-clock phase delay, and an area of approximately 0.09 μm^2. From these results, it is seen that the proposed Full Adder is optimized compared to the previous one.

V. Conclusion

In this letter, an optimized QCA full comparator was proposed. The proposed comparator is simulated using the QCADesigner tool, and the simulation results show that the logical function of the designed circuit is correct. The optimized QCA full comparator shows improvement in terms of area, cell count, and delay. In comparison with the best previous full comparator, our design has 64% and 85% improvement in the cell count and the area, respectively. Also, our comparator is faster than previous ones. Therefore, the implementation of this design may lead to the efficient use of calculative units in various applications, which may be used as a basic building block of a general purpose nano processor.

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