CMOS Active Inductor: A Technical Review

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Abstract: The demand of configurable and compact RF integrated circuit is ever increasing since the inception of CMOS technology. The inductor has been an essential component in RF system design blocks such as voltage controlled oscillator, low noise amplifier, matching network, filter, power divider, power supply noise reduction etc. The gyrator-C based CMOS active inductor is recent research topic because of its tunability, compactness and high quality factor. This paper presents the detailed review of gyrator-C based CMOS active inductor and several techniques to enhance its performance.

Keywords: Active Inductor (AI), Complementary Metal Oxide Semiconductor (CMOS), Gallium Arsenide (GaAs), Gyrator, Noise, Metal–semiconductor field-effect transistor (MESFET), Radio frequency (RF), Transconductors, Quality factor (Q).

INTRODUCTION

Inductors are prominent element in RF circuit design [1]. Fig. 1 illustrates LC-voltage controlled oscillator where spiral inductors consume the dominant chip area. The other drawbacks of spiral inductor are fix inductance value and weak quality factor, which are the main constraints in RF integrated circuit design [2]. Over that, advantages of active inductors are small chip area, high quality factor, wide inductive bandwidth and low voltage operation [3].

The most vital advantage of active inductor over passive counterpart is its tunability. Nevertheless, active inductor has certain drawbacks as power consumption, noise, poor linearity - all these are inherent in active inductor circuit [4]. The Gallium Arsenide (GaAs), Metal Semiconductor Field-Effect Transistor (MESFET) and bipolar technologies are the alternative techniques to realize an active inductor. But the CMOS active inductor has proven the greatest achievement towards the inexpensive chip design [5].
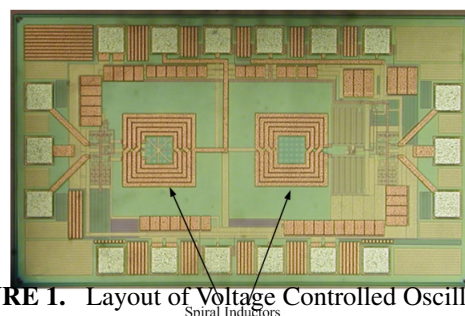

FIGURE 1. Layout of Voltage Controlled Oscillator [6].

The organization of paper is as follows. The basic active inductor topology is described in Section 2. The various active inductor architectures are presented in Section 3. Finally, Section 4 summarizes the technical review.

BASIC PRINCIPLE

The impedance of an ideal inductor is described by the signal flow graph (SFG) as illustrated in Fig. 2, where s is the laplace operator and L is the inductance of the inductor.

$$\frac{V_{in}}{I_{in}} = sL \tag{1}$$
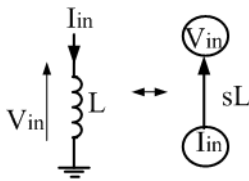
FIGURE 2. An ideal inductor and its SFG representation [7].

The same transfer function can be obtained by using one capacitor and two trans-conductance (one positive and one negative) amplifiers as shown in Fig. 3 called as **gyrator-C** network.
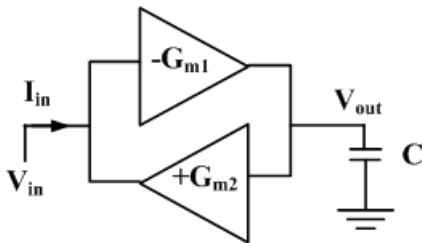
FIGURE 3. Gyrator-C based ideal active inductor [7].

Considering I_{in} and V_{in} as current and voltage at input node, resultant impedance can be derived as:
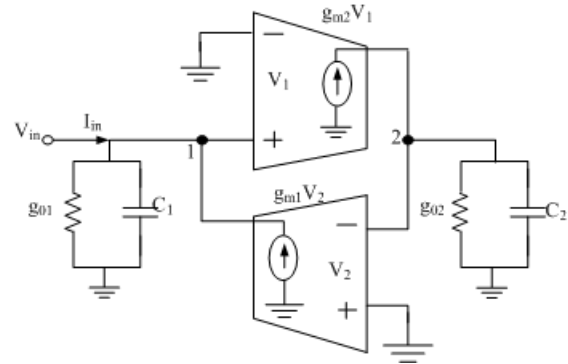
$$\frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}} \tag{2}$$

The consequence of Eq. (1) and (2) follows:

$$L = \frac{C}{G_{m1}G_{m2}} \tag{3}$$

Single and Double Ended Active Inductor

The single ended and double (differential) ended active inductors are the basic classification of active inductors. In both the cases AI is lossless only when the input and output

FIGURE 4. Lossy single ended active inductor [8].

impedances of the transconductors are infinite and their trans conductance is constant, that is practically impossible. Henceforth, the equivalent impedance for the lossy gyrator-C can be derived as,

$$\frac{V_{in}}{I_{in}} = \frac{1}{sC_2 + G_{02} + \frac{G_{m1}G_{m2}}{sC_1 + G_{01}}} \tag{4}$$

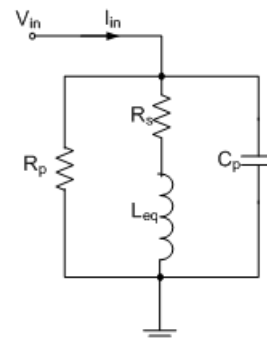Simplification results into the following equivalent terms:

$$C_p = C_2 \tag{5}$$

$$R_p = \frac{1}{G_{02}} \tag{6}$$

$$L_{eq} = \frac{C_1}{G_{m1}G_{m2}} \tag{7}$$

$$R_s = \frac{G_{01}}{G_{m1}G_{m2}} \tag{8}$$

Where (g_{m1} and g_{m2}) are transconductances, (g_{01} and g_{o2}) are output conductances and $C_1 - C_2$ are the parasitic capacitances at node 1 and 2 respectively.

Subsequently, it can work as resonator as presented in Fig. 5.

FIGURE 5. Equivalent electric model of active inductor in Fig. 3 [8].

In similar way, differential active inductor and its simplified resultant circuit are shown in Fig. 6 and 7, respectively.
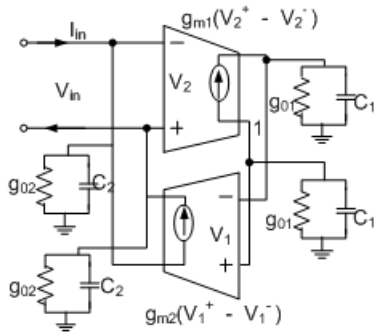

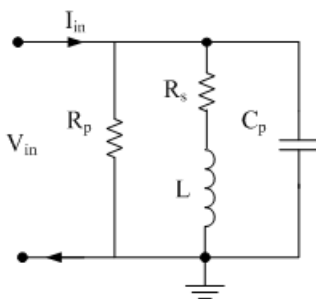**FIGURE 6.** Lossy differential active inductor [**?**].

FIGURE 7. Equivalent electric model of active inductor in Fig. 6 [8].

To acquire the inductive behaviour ac analysis is required that gives the performance of circuit as shown in Fig. 8. The frequency range between ω_z and ω_o is the main area of interest. Recently, researchers are working towards enhancement of this inductive range with high quality factor and optimum noise, linearity, area and power consumption.

ACTIVE INDUCTOR ARCHITECTURES

CS-CD based Gyrator-C

Ismail proposed first CMOS based active inductor as manifested in Fig. 9. It is composed of common source (M_1) as negative transconductor and common drain (M_2) as positive trans conductor. The internal gate-to-source/drain capacitance of the MOS transistor performs as capacitance at node 1 and 2, respectively.
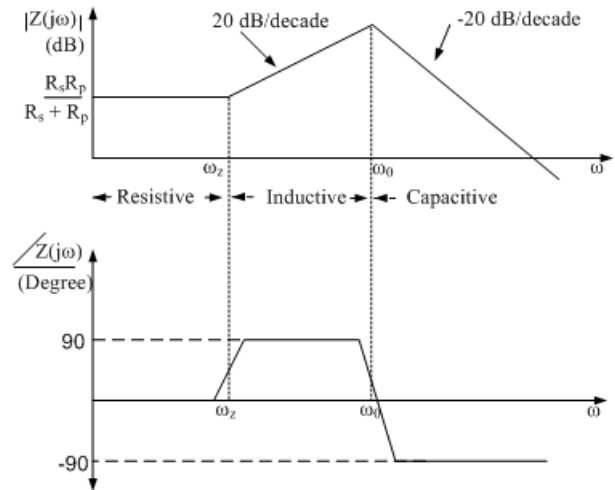

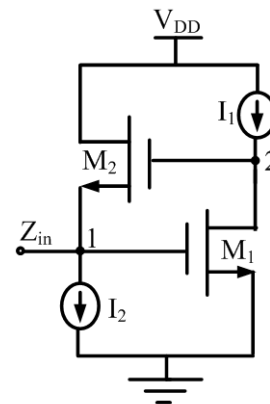**FIGURE 8.** Bode plot of active inductor [**?**].

FIGURE 9. Basic Gyrator Circuit [9].

Common Drain stage has encountered greater restrictions on the voltage levels required to properly bias the transistors, which has a negative impact on the inductance tuning range. Alternative way to enhance the inductance tuning range is a cascode stage.

Cascode Active Inductor

The cascode topology is effective to reduce the output conductance and subsequently lowering the series resistance. Fig. 10 shows the cascode active inductor. Though cascode topology achieves higher inductance and quality factor, it limits dynamic range and it is not compatible with low voltage ($<= 1.8\,\text{V}$) operation.
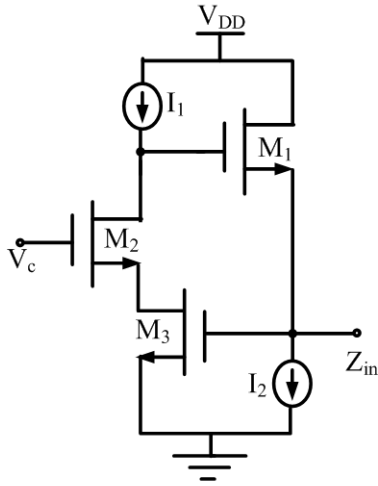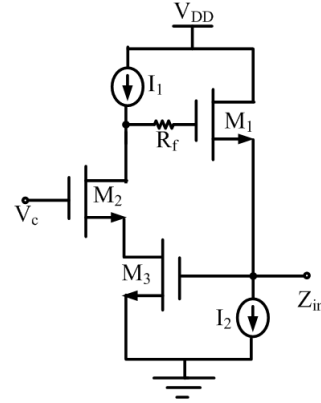
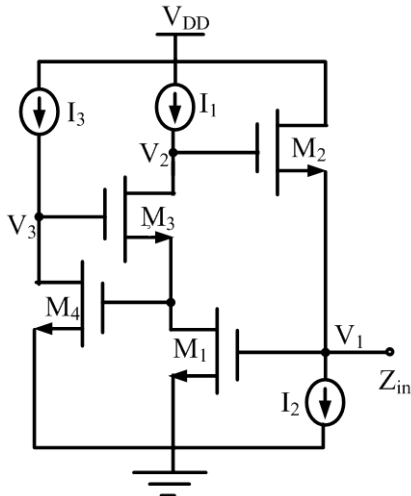**FIGURE 10.** Cascode Active Inductor [10].

FIGURE 11. Regulated Cascode Active Inductor [10].

Regulated cascode active inductor

In order to tune inductance and quality factor individually, regulated cascode is used as presented in Fig. 11. Addition of feedback amplifier (M_4) to regulate the gate of M_3 further reduces the output conductance g_{01} and its is controlled by I_3.

Resistive Feedback Active Inductor

Addition of feedback resistance R_f ensures the improvement in cascade gain . As exhibited in Fig. 12, the feedback resistance R_f forms an additional inductive reactance which significantly increase the inductance. To make the circuit tunable, resistance R_f can be implemented using

a PMOS transistor in the triode region. By varying the gate drain control voltage of the PMOS transistor, the inductance can be varied.

FIGURE 12. Resistive feedback in Active Inductor [11].

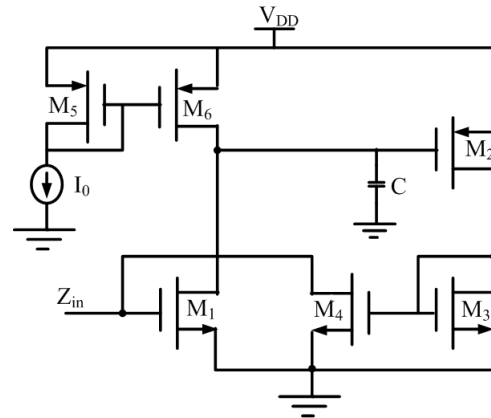**High Quality factor active inductor**

FIGURE 13. High-Q Active Inductor [4].

Fig. 13 and 14 are composed of two trans conductors realized by MOS transistors in common source configuration connected in feedback. The common source facilitates low conductance at critical nodes (Z_{in} and Z_{out}). Henceforth, it provides high-Q factor.

Low noise active inductor

In context to this circuit, differential configuration (positive transconductor) makes the entire circuit less sensitive to noise. Fig. 15 presents two approaches: (i) usage of PMOS cascode and (ii) differential configuration using only NMOS transistors. It results in the circuit having high inductive bandwidth and low noise.
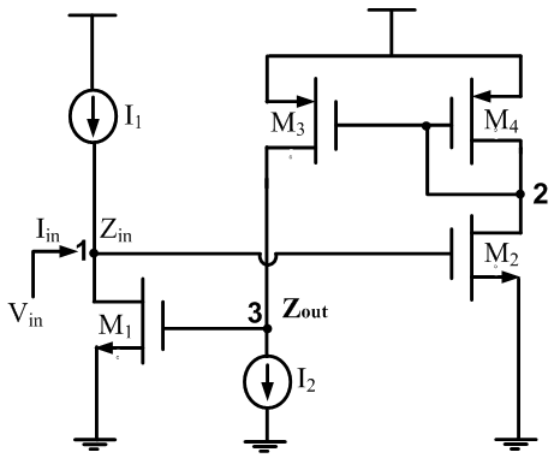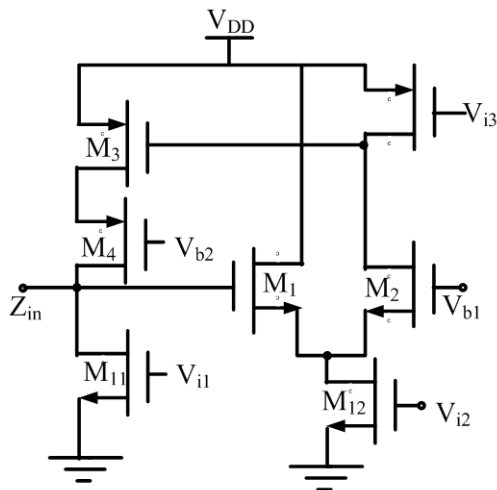
FIGURE 14. High Active Inductor [12].

FIGURE 15. low noise Active Inductor [13].

FIGURE 16. High frequency Active Inductor [14].

FIGURE 17. Cascode Active Inductor [15].

but the higher value of parasitic series resistance and lower value of parallel resistance value provide the lower value of quality factor.

CONCLUSION

This paper presents intense review of gyrator based CMOS active inductor. The several techniques are used to enhance the performance of active inductor. As per the application requirement the active inductor circuit can be used.

High frequency active inductor

It is known that the mobility of NMOS is around four to five times greater than PMOS in submicron CMOS technology. Although the P channel transistors help to reduce noise and nonlinearity in the circuit, the high frequency performance of active inductor is possible only by using NMOS transistors as shown in Fig. 16. That increases the operating frequency significantly.

Low power Active Inductor

Recently common gate- common source gyrator based active inductor has been discussed in [15] as depicted in Fig. 17. Less number of transistors proves the small chip area and low power consumption of active inductor circuit
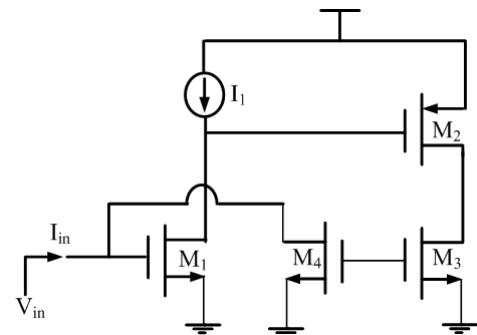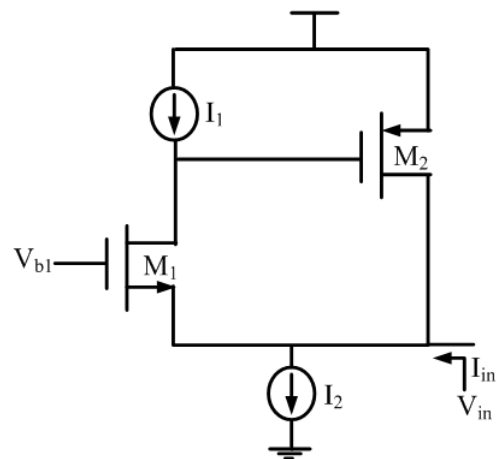
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