Sampling Circuits That Break the kT/C Thermal Noise Limit

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***Abstract*—Several circuit-level techniques are described which are used to reduce or cancel thermal noise and break the so-called kT/C limit. kT/C noise describes the total thermal noise power added to a signal when a sample is taken on a capacitor. In the first proposed technique, the sampled thermal noise is reduced by altering the relationship between the sampling bandwidth and the dominant noise source, providing a powerful, new degree of freedom in circuit design. In the second proposed technique, thermal noise sampled on an input capacitor is actively canceled using an amplifier, so that the noise at the amplifier output can be controlled independently of input capacitor size. Measurements from two test chips are presented which demonstrate sampled thermal noise power reduction of 48% and 67%, respectively, when compared with conventional kT/C-limited sampling.**

***Index Terms*—Auto-zero, correlated double sampling, Johnson noise, kT/C, sampling, switched-capacitor, track-and-hold, thermal noise.**

I. Introduction

SWITCHED-CAPACITOR circuits are the implementation of choice for many modern mixed-signal circuits, especially in CMOS technology. Inherent in any switched-capacitor circuit are sampling operations; when a switch opens, freezing the charge on a capacitor, a sample is taken. In conjunction with amplifiers, the sampled charge can then be redistributed to other capacitors in order to implement a variety of circuit functions: buffers, gain blocks, filters, and data converters [1], [2]. At the circuit design level, one of the common issues with sampling is the addition of noise to a signal each time a sample is taken. This noise represents a major limitation on the performance of most switched-capacitor circuits.

While capacitors are noiseless circuit elements, the resistors or transistors used to transfer charge contribute noise. Typically, when considering the noise associated with sampling, thermal noise is the dominant noise source. Thermal noise, which is also called Johnson or Nyquist noise, occurs due to the random motion of carriers due to thermal agitation. Unlike many other noise sources, such as shot noise and flicker noise, thermal noise occurs in the absence of dc current flow. Therefore, even with a dc input and a sampling circuit that has reached thermal equilibrium, thermal noise will be present and limit the achievable signal-to-noise ratio (SNR). It should be noted that flicker noise can also be a significant noise contributor in switched-capacitor circuits, particularly in the case of active circuits. However, noise that is slow-moving relative to the sample rate can be reduced or eliminated using offset-cancellation techniques, such as an auto-zero configuration [3] and amplifier chopping [4], [5].

Focusing on the most basic example, a sample taken on a single capacitor C with a transistor acting as a switch, it can be shown that the total thermal noise power on the sampling capacitor is equal to kT/C, where k is the Boltzmann constant, T is absolute temperature, and C is the sampling capacitance. While the details of the kT/C limit will be discussed in Section II, there are significant implications of this limit. Specifically, in order to achieve lower noise in a sampled system, larger capacitors must be used. Unfortunately, when increasing capacitor size in order to lower noise, other performance parameters suffer. The impacts can include larger die area, higher power in the sampling stage, and higher power in the amplifier that drives these increased sampling capacitors. It would be desirable to possess an extra degree of freedom with which the sampled noise could be designed independently of sampling capacitor size. This paper will discuss two techniques that enable such a design degree of freedom [6].

The remainder of this paper is organized as follows. Section II includes background information. Section III describes the use of negative feedback and bandlimiting to reduce sampled thermal noise. In contrast, Section IV describes an active noise cancellation technique. Measurement results demonstrating each technique are included in the corresponding sections.

II. Background

A. kT/C Noise

The total thermal noise power on a capacitor in parallel with a single resistor was first shown in [7] to reduce to the familiar kT/C limit, using the equipartition theorem of thermodynamics. The analysis can be extended to a very simple track-and-hold sampling circuit, shown in Fig. 1. Assuming that the sampling transistor is operating in the triode region with a small voltage potential between the drain and source, it can be represented by an equivalent noise generator whose noise power spectral density is equal to $4kTR_{\mathrm{ON}}$ [$\mathrm{V^2/Hz}$], where k is again the Boltzmann constant, T is absolute temperature, and R_{ON} is the on-resistance of the sampling switch [8]. While this is equivalent to the circuit analyzed in [7], an alternative analysis uses Parseval's theorem to calculate the total thermal noise power on the sampling capacitor

$$\overline{\mathrm{v_n^2}} = (4\mathrm{kTR_{ON}}) * \int_0^\infty \left| \frac{1}{1 + \mathrm{j}2\pi \mathrm{fR_{ON}C}} \right|^2 \mathrm{df}. \qquad (1)$$

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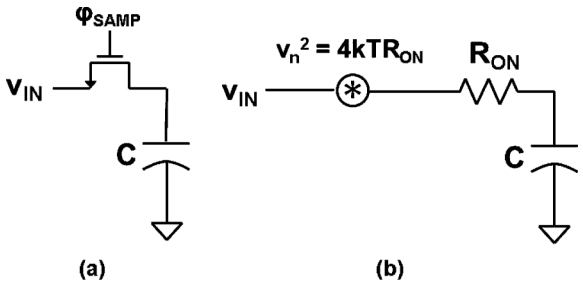

Fig. 1. Basic sampling circuit. (a) Single transistor as sampling switch. (b) Equivalent noise circuit during track phase.

For a simple single-pole system, such as Fig. 1, it is often easiest to reduce the integral into an equivalent noise bandwidth (ENBW) and to then express the total noise power as the product of the noise power spectral density and the ENBW as follows:

$$\mathrm{ENBW} = \int_0^\infty \left| \frac{1}{1 + j2\pi \mathrm{fR_{ON}C}} \right|^2 \mathrm{df} = \frac{1}{4\mathrm{R_{ON}C}} \tag{2}$$

$$\overline{\mathrm{v_n^2}} = (4\mathrm{kTR_{ON}}) * \frac{1}{4\mathrm{R_{ON}C}} = \frac{\mathrm{kT}}{\mathrm{C}}. \tag{3}$$

In this simple case, the value of the transistor on-resistance $(\mathrm{R_{ON}})$ appears in both the numerator (noise power spectral density) and the denominator (equivalent noise bandwidth). Therefore, the on-resistance terms cancel, and only the sampling capacitor remains as a degree of freedom in the expression for total noise power. This same "canceling" relationship is found to hold for more complicated structures as well, such as amplifiers in feedback that are used to provide a virtual ground for sampling.

The cancellation can be easily seen when the noise power spectral density sampled on the capacitor is plotted versus frequency, as in Fig. 2. A lower transistor on-resistance decreases the thermal noise density, but the noise bandwidth is increased by the same ratio. There is no obvious way to decouple the inverse proportional relationship between the noise power density and the noise bandwidth. The noise reduction technique proposed in Section III specifically addresses this inverse relationship.

The distinction between sampling bandwidth (or ENBW) and sample rate should be made clear and is also shown in Fig. 2. Here, the track-mode ENBW, f_{track}, is shown to be significantly larger than the sampling frequency, f_s. In order to achieve good linearity, track-mode or settling bandwidth is often designed to be at least $0.25(N + 1)$ higher than the sampling frequency, where N is the number of bits of accuracy, and may be even higher in a sub-sampled system [9]. However, the total sampled thermal noise is determined only by the noise spectral density and the equivalent noise bandwidth, and is not affected by the sample rate. Therefore, the remainder of this paper will refer only to equivalent noise bandwidth and not sampling frequency.

B. Prior Thermal Noise Reduction Work

Historically, image sensors such as CCDs have been very sensitive to kT/C noise. One of the first techniques developed to mitigate the effect of thermal noise in image sensors was called correlated double sampling [10]. This technique is effectively a cancellation of thermal noise associated with a reset transistor, and a functional diagram is shown in Fig. 3. The key concept of this technique is that the thermal noise from the reset transistor, once sampled on capacitor $\mathrm{C_S}$, will remain constant. Therefore, two readings of the pixel output can be taken, one just after the reset switch opens, and a second after the photocurrent has been integrated. Because the reset noise, v_{ns} is correlated between these two readings, the final differenced output is independent of the sampled thermal noise from the reset switch. While the reset of a CCD pixel is a rather limited application, the concept of removing correlated noise is powerful.

More recently, several techniques have been proposed for CMOS image sensors that actively reduce reset transistor noise [11]–[13]. The details of these techniques differ, but they operate on similar principles. A negative feedback loop is wrapped around the reset transistor, including an amplifier that controls one of its terminals. At frequencies for which the feedback loop has gain, the noise of the reset transistor is reduced by the negative feedback, typically requiring the bandwidth of the pixel reset to be limited. This is a compromise that can be tolerated in image sensors with relatively long reset times. Often, the bandwidth of the amplifier itself must also be restricted by using some auxiliary large capacitor; however, the amplifier and auxiliary capacitor do not reside inside the individual pixels, so the power and area penalty incurred are acceptable.

In contrast to these techniques that have been developed to counteract reset noise in image sensors, the circuits proposed in the following sections reduce or cancel sampled thermal noise while also being able to sample an arbitrary and time-varying input voltage. Also, because the proposed circuits include amplifiers, they are able to implement active switched capacitor functions, such as voltage gain or filtering.

III. Noise Reduction Via Feedback

A. Circuit Configuration

In order to reduce sampled thermal noise without increasing sampling capacitance, the relationship between the dominant noise source and the impedance which limits the noise bandwidth must be broken. This can be accomplished with the feedback circuit configuration proposed in [14] and shown in Fig. 4. This configuration is very similar to a conventional offset-canceling auto-zero configuration [15]. It consists of a transconductance amplifier G_M connected in negative feedback to provide a virtual ground against which the capacitor is sampled. The amplifier is resistively loaded and, unlike the conventional auto-zero, includes an explicit large feedback resistance R_{FB}.

Conceptually, the effect of R_{FB} during track mode can be understood by considering the path that current takes when flowing out of the transconductance amplifier. At low frequencies, the impedance of the sampling capacitor C_S is very large, and therefore most of the current output from G_M will flow through R_L to ground, which is no different than a conventional auto-zero. However, at high frequencies, the impedance of C_S is small, and current output from G_M will split between the feedback and load paths, as compared to a conventional configuration in

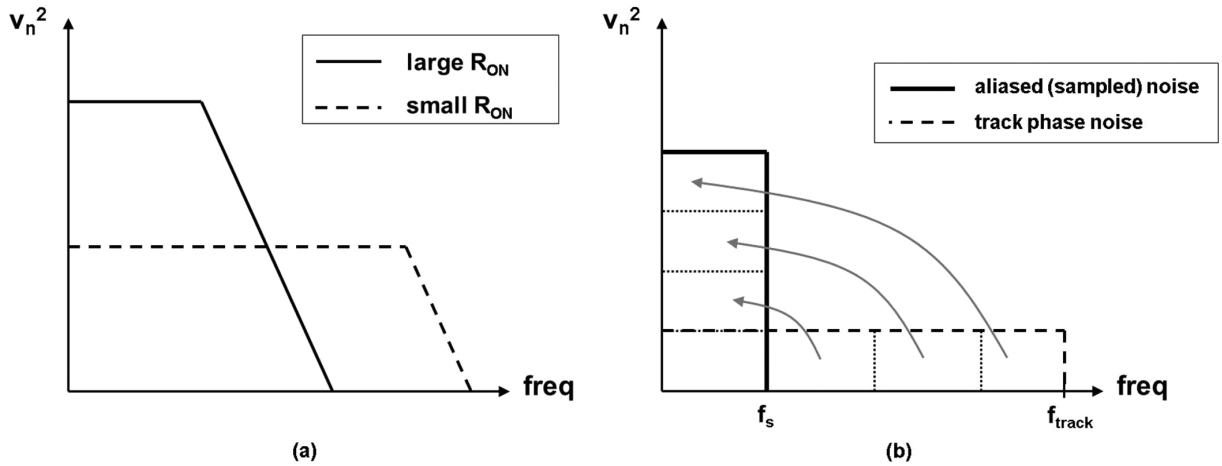

Fig. 2. Noise power spectral density. (a) Impact of different sampling switch resistance. (b) Impact of aliasing due to sampling.

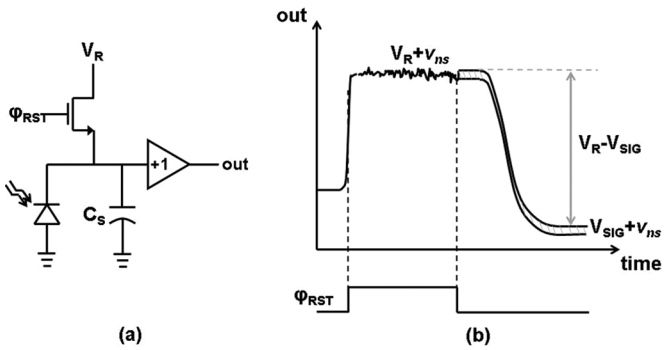

Fig. 3. Correlated double sampling. (a) Functional diagram of CCD pixel, including reset transistor. (b) Pixel output versus time, including noise from reset transistor.

which all of the amplifier current would flow through the feedback path. The current split is determined by the ratio of feedback and load resistors, and its effect is to reduce the high-frequency effective feedback path transconductance

$$\mathrm{G_{M,EFF}} = \mathrm{G_M}\frac{\mathrm{R_L}}{\mathrm{R_L}+\mathrm{R_{FB}}}. \tag{4}$$

As shown, $G_{M,\mathrm{EFF}}$ provides a new degree of freedom; namely, it can be adjusted independently of G_M by adjusting the ratio between R_L and R_{FB}. This is precisely the decoupling of dominant noise source (amplifier G_M) and bandwidth limiting impedance ($G^{-1}_{M,\mathrm{EFF}}$) required in order to achieve integrated noise power lower than kT/C.

B. Feedback Analysis

An equivalent feedback block diagram, also shown in Fig. 4, can be analyzed to more rigorously understand the dynamics and noise contributions of the proposed configuration. This block diagram also includes the addition of two noise sources. Current noise, added at the amplifier output, is used to model amplifier noise. The noise contribution of the feedback resistor is modeled as a voltage noise that is added in series with the amplifier output voltage. Expressions for the impedance at the output node Z_{OUT}, feedback factor β, and loop transfer function $L(s)$ can be derived as

$$\mathrm{Z_{OUT}} = \frac{\mathrm{R_L}(\mathrm{R_{FB}C_S}s+1)}{(\mathrm{R_L}+\mathrm{R_{FB}})\mathrm{C_S}s+1} \tag{5}$$

$$\beta = \frac{1}{\mathrm{R_{FB}C_S}s+1} \tag{6}$$

$$\mathrm{L(s)} = \frac{\mathrm{G_M R_L}}{(\mathrm{R_L}+\mathrm{R_{FB}})\mathrm{C_S}s+1}. \tag{7}$$

The loop transfer function is a single pole expression, so that unity gain frequency (UGF), and hence closed-loop bandwidth of the system, can be easily seen and rewritten as a function of the effective loop transconductance

$$\mathrm{UGF} = \frac{\mathrm{G_{M,EFF}}}{\mathrm{C_S}} \tag{8}$$

As expected, the loop bandwidth, which is also the sampling bandwidth, is directly proportional to $G_{M,\mathrm{EFF}}$. Finally, the transfer function from the amplifier current noise to the voltage on the sampling capacitor and the total noise from the amplifier are

$$\frac{\mathrm{v_{sum}}}{\mathrm{i_{n,amp}}} \approx \frac{1}{\mathrm{G_M}} * \frac{1}{\frac{\mathrm{C_s}}{\mathrm{G_{M,EFF}}}s+1} \tag{9}$$

$$\overline{\mathrm{v^2_{n,amp}}} = \gamma\frac{\mathrm{kT}}{\mathrm{C_S}} * \frac{\mathrm{R_L}}{\mathrm{R_L}+\mathrm{R_{FB}}}. \tag{10}$$

The above equations are written in terms of the effective loop transconductance and are slightly simplified by making the assumption that the open-loop gain of the amplifier $G_M R_L$ is much greater than unity. Compared with a conventional configuration, the dc component of the amplifier noise transfer function is the same as conventional configuration, G_M^{-1}. The bandwidth of the amplifier noise, however, is determined by the sampling capacitor and the effective transconductance, confirming that the inclusion of the feedback resistor indeed provides a method to control the total thermal noise. Note that the additional term γ in (10) is an amplifier noise factor and accounts for noise contributions from amplifier devices other than the input

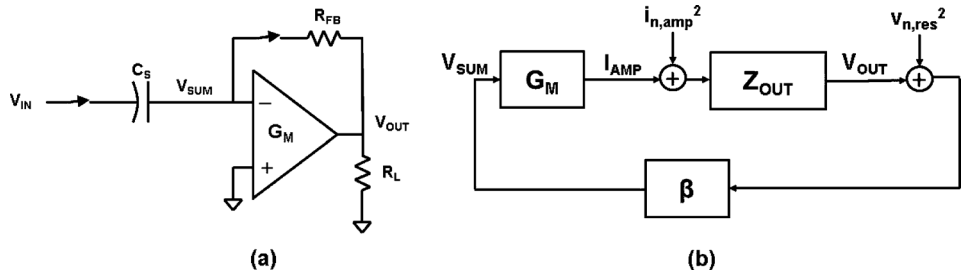

Fig. 4. Feedback configuration for reducing sampled thermal noise. (a) Circuit diagram with nodes labeled, switches shown closed as during track phase. (b) Feedback block diagram, including addition of noise sources.

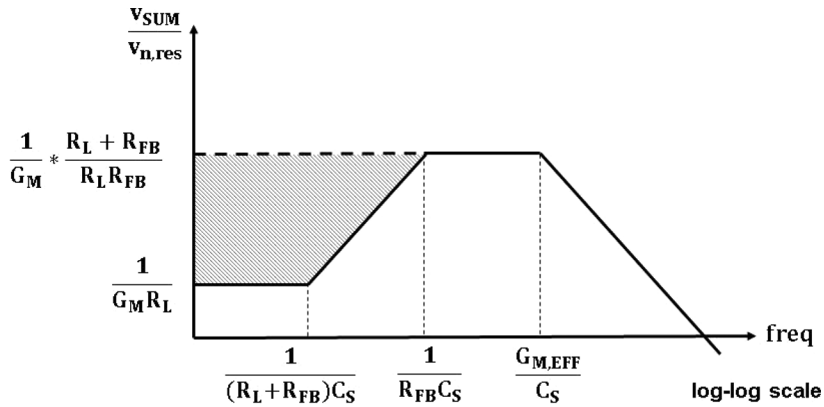

Fig. 5. Feedback resistor noise transfer function to sampling capacitor.

differential pair, as well as any potential excess thermal noise in the input devices themselves.

Of course, it is also important to consider the noise from $R_{\rm FB}$, which is typically a rather large resistance and therefore might be expected to have a large noise contribution. The transfer function from the feedback resistor voltage noise to the sampling capacitor is

$$\frac{\rm v_{sum}}{\rm v_n} \approx \frac{1}{\rm G_M R_L + 1} * \frac{\rm (R_L{+}R_{FB})C_S s + 1}{(R_{\rm FB}C_S s + 1)\left(\frac{\rm C_s}{\rm G_{M,EFF}} s + 1\right)}. \quad (11)$$

This transfer function, plotted in Fig. 5, has a zero and two poles, and hence it is difficult to define an equivalent noise bandwidth. However, the analysis can be simplified by approximating the transfer function as flat to dc, shown as the dotted line in Fig. 5. This approximation is pessimistic; the noise gain for frequencies below the first pole will be increased as shown in the shaded gray area. It should be noted that as $R_{\rm FB}$ is increased relative to R_L, a condition which reduces amplifier noise as shown in (10), the transfer function shown in Fig. 5 approaches the dotted line approximation. As such, the approximate integrated noise due to the feedback resistor is

$$\overline{\rm v_{n,res}^2} = \frac{\rm kT}{\rm C_S} * \frac{1}{\rm G_{M,EFF} R_{FB}}. \quad (12)$$

Finally, all of the noise contributions can be combined as follows:

$$\overline{\rm v_n^2} = \frac{\rm kT}{\rm C_S} * \left(\frac{\gamma \rm R_L}{\rm R_L + R_{FB}} + \frac{1}{\rm G_M R_L} + \frac{1}{\rm G_M R_{FB}}\right). \quad (13)$$

From (13), it is clear what conditions are needed to achieve sampled thermal noise less than kT/C. The first term in (13) represents the amplifier noise and, to reduce it, large $R_{\rm FB}$ is desired. The second term is due to feedback resistor noise and is kept small if the amplifier dc gain $G_M R_L$ is large. Finally, the third term, due to load resistor noise, has not been discussed, but the analysis is similar to feedback resistor noise. The impact of this noise source is also minimized with a large $R_{\rm FB}$.

Increasing $R_{\rm FB}$ does not come without a price, however. As can be seen in (4) and (8), increasing $R_{\rm FB}$ decreases the sampling bandwidth. If it is desirable to maintain a wide sampling bandwidth while decreasing noise, then G_M must be increased as $R_{\rm FB}$ is increased, resulting in increased power. It should be noted that increasing power to reduce noise is not a penalty specific to this technique. With the conventional sampling method, the sampling capacitor would be increased in order to decrease noise, requiring increased power in the driving circuit in order to keep the bandwidth constant.

C. Source Noise

The previous sections analyzed the noise contributed by the sampling circuit, including the amplifier and feedback resistor. To account for all of the noise that will be sampled on the sampling capacitor, the noise density of the source must also be considered.

In analysis of conventional sampling, such as in Fig. 1, the source impedance is often ignored. If the source behaves as an ideal impedance, this simplification is appropriate; the source impedance can simply be lumped together with the switch resistance, and it has already been shown that the sampled thermal noise is independent of switch resistance. However, if the source is driven by an amplifier or buffer circuit, it is often the case that its noise spectral density is larger than would be expected when

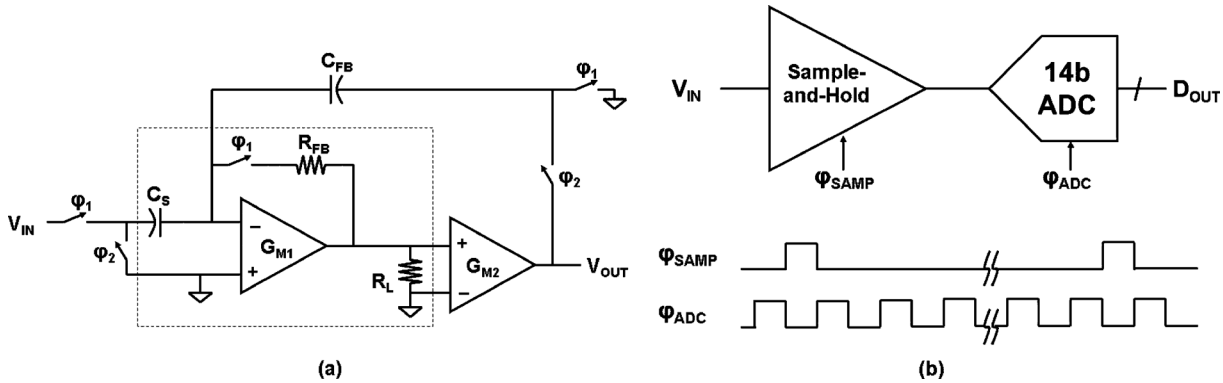

Fig. 6. Implementation of noise reduction technique in track-and-hold amplifier. (a) Circuit diagram. (b) Use of track-and-hold in signal chain with an ADC, including clock timing diagram.

considering its output impedance. In this case, it is most convenient for the designer to consider the source noise power density integrated over the entire sampling bandwidth. This total noise can be greater than kT/C, and care must be taken in the design of the source to ensure that its noise spectral density is adequately low.

Exactly the same considerations apply for the circuit proposed in Fig. 4. Source noise is indistinguishable from the input signal, and it is integrated over the entire sampling bandwidth. Unlike its effects on amplifier and feedback resistor noise, the feedback configuration does nothing to actively reduce source noise. Its effect is to control the sampling bandwidth, and in a manner that can be independent of sampling capacitance. Care must still be taken in the design of the source to ensure that its noise spectral density is adequately low for the given sampling bandwidth. It should also be noted that the left-most switch in Fig. 4(a) is effectively in series with the source impedance; as such, its on-resistance should be sufficiently low so as to not dominate the total noise sampled.

Finally, while the proposed technique does not fundamentally ease the design of the source driver, in practice there are usually benefits to shrinking the sampling capacitor. Smaller capacitors, in addition to occupying less chip area, typically require less sprawling interconnect and can often be driven by smaller switches. The reduced parasitics associated with both of these benefits can translate into significant power and complexity reduction, particularly if auxiliary functions such as clock-bootstrapping are being used.

D. Prototype Implementation

The proposed technique has been used as the pre-amplifier stage of a track-and-hold amplifier, as shown in Fig. 6 [14]. The technique is well suited for low- to medium-gain wideband applications, such as this pre-amplifier. In this implementation, the gain is relatively low, 16 dB, and the load resistor is 330 Ω. The feedback resistor is 1 kΩ. Parasitics at the pre-amplifier output node do not have significant impact on stability, even with a closed-loop bandwidth greater than 300 MHz. Given these component values, (13) predicts that the sampled thermal noise power should be 1/2 of the kT/C_S limit.

The track-and-hold circuit is followed by a 14-bit ADC in the signal chain also shown in Fig. 6. The clocks applied are designed to measure only the input sampling noise through the use of oversampling. A single input sample is taken, as shown by clock φ_{SAMP}. This input is then held for multiple ADC conversions. The ADC outputs are averaged together, which reduces the error introduced by amplifier hold noise and ADC noise, resulting in an accurate estimate of the single input sample. For these measurements, each input sample is converted several thousand times by the ADC, reducing the effective measurement noise to less than 5 μV-rms.

A test chip that includes the circuit shown in Fig. 6 has been fabricated in a 0.18 μm CMOS process. The ADC clock rate is 40 MSPS. The size of the sampling capacitor is 2.4 pF. Additional capacitance at the summing node, due to C_{FB} and some other parasitic capacitance, totals 1.5 pF. Based on (13), and accounting for the impacts of a differential implementation and parasitic capacitance, the kT/C-limited sampled thermal noise should be 75 μV-rms. The test chip includes a mode in which the auto-zero is disabled and the input is sampled in conventional fashion with a sampling switch at the summing node (not shown in Fig. 6).

Fig. 7 shows data measured on test chip #1 in two configurations. The gray histogram corresponds to conventional sampling, and the measured standard deviation is 72 μV-rms. The black histogram is the same circuit configured in noise-reducing feedback mode. The measured standard deviation drops to 52 μV-rms. The difference between the two sets of data represents a 48%, or 2.8 dB, reduction in noise power. There are plenty of sources of difference between measured and predicted data, including uncertainty in the size of the fabricated sampling capacitor. However, because all measurements were taken on the same chip, variations in circuit elements should not impact the accuracy of the noise power reduction measured. It should also be noted that this test chip is a modification of a previous design, in which the only significant change is the addition of the feedback resistor. As such, it can be said that the thermal noise reduction essentially comes for free, with, of course, the exception of reduced track-mode bandwidth as described in Section III-B.

A spectrum of the measured output data is shown in Fig. 8. Note that the sample rate has been decreased to 6 MSPS for this data, so that the low frequency portion of the spectrum is clearly visible. For this measurement, the sampling clock and ADC clock are identical. Because the system is no longer oversampled, it is impossible to separate the noise contributions

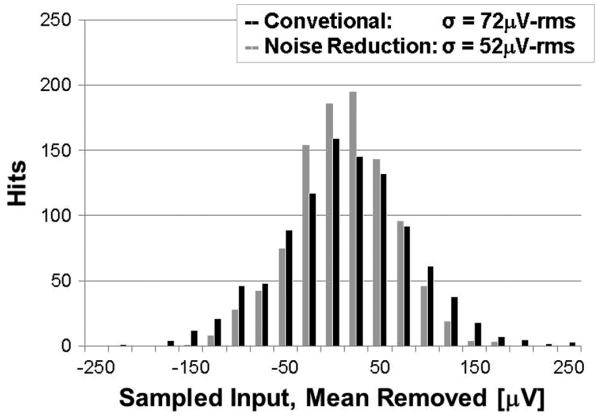

Fig. 7. Measured histograms for 1000 input samples on test chip #1, with mean value removed.

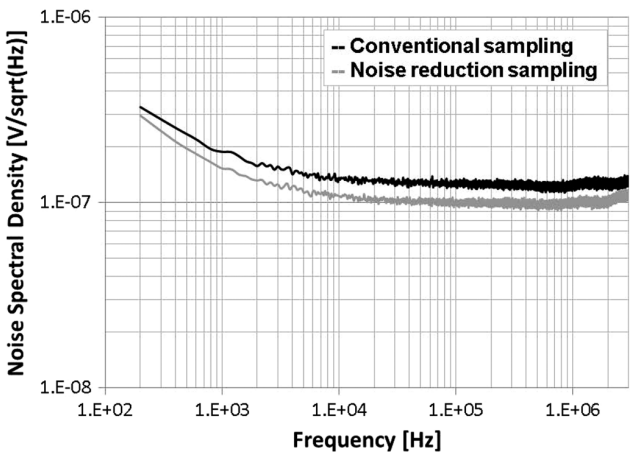

Fig. 8. Spectrum of measured data for 6 MSPS sample rate, with and without noise reduction enabled.

from input sampling, amplifier hold, and A-to-D conversion. This is the reason for the colored spectrum; 1/f noise in the track-and-hold second stage as well as in the ADC dominates the noise spectrum at low frequencies. This plot shows that the thermal noise floor drops by ∼15% when the noise reduction is enabled. This decrease is not as dramatic as the data in Fig. 7, due to the inclusion of amplifier hold and A-to-D conversion noise. When all of the contributions are accounted for, the results are consistent.

IV. Active Noise Cancellation

A. Circuit Configuration

While the noise reduction technique described in the previous section focused on reducing the thermal noise sampled, the technique proposed here will instead use active circuits to cancel the thermal noise after it has already been sampled. An implementation of this technique is shown in Fig. 9. The circuit blocks shown comprise a track-and-hold built using a two-stage amplifier with capacitive level-shifting between the two stages. As in Fig. 6, the first amplifier A_1 is typically a low-gain pre-amplifier stage, though the technique would also work with a higher gain first stage.

Noise cancellation is achieved through appropriate design of the switch controls shown in Fig. 9(b). During the input sampling phase, both signals φ_1 and φ_2 are active (high). In this phase, the input voltage $V_{\rm IN}$ is stored on input capacitor C_S, the offset of amplifier A_1 is stored on auxiliary capacitor C_2, and feedback capacitor $C_{\rm FB}$ is cleared. When φ_1 falls, the charge on the input and feedback capacitors is frozen. Thermal noise charge is also sampled with noise power equal to $kT/(C_S + C_{\rm FB})$. Operation in this phase is identical to an output-referred auto-zero [3]. This is also sometimes referred to as correlated double sampling [16], though the term's use as an offset cancellation technique can be confused with the application to reset noise cancellation [10], and is hence referred to herein as auto-zero.

After $\varphi 1$ falls, thermal noise on C_S is sampled and the summing node will settle to a final, noisy voltage. This voltage is amplified through A_1 and stored on capacitor C_2, as signal φ_2 is still active. When φ_2 falls, the sampled voltage on capacitor C_2 captures both the offset of amplifier A_1 and an amplified version of the thermal noise that was sampled at the summing node. Effectively, both offset in A_1 and the sampled thermal noise at the summing node will be auto-zeroed out via the same mechanism during phase φ_3.

During φ_3, the circuit is configured in hold mode and the input charge is transferred from C_S to $C_{\rm FB}$. However, the noise charge sampled on C_S is not transferred to $C_{\rm FB}$ and therefore does not appear at the amplifier output. To demonstrate that the noise charge is not transferred, it is easiest to begin with the assumption that A_2 has infinite gain. Therefore the feedback loop will settle with no signal at the input to A_2. If the right-hand side of C_2 has no signal, then the left-hand side of C_2 and the summing node must remain at the same potential as they were when φ_2 sampled. Therefore, the sampled thermal noise charge stays on the summing node and is not transferred to $C_{\rm FB}$. A similar analysis can be used to show that the offset of A_1 also does not appear at the amplifier output.

It is also important to consider thermal noise sampled on capacitor C_2, as this noise is not cancelled during φ_3. The sampled thermal noise power on C_2 is proportional to kT/C_2. One obvious way to decrease this noise contributor is to increase capacitor C_2. While this increase may seem not desirable, C_2 is not driven by the input, and decreasing C_S at the expense of increased C_2 is often a favorable trade-off. Another approach to decreasing the noise contribution from the C_2 sample is to increase the gain of A_1, which lessens the impact of this noise when referred back to the input. The challenges with these approaches will be discussed next.

B. Impact on Sampling Bandwidth

A practical limitation that must be considered is the time required for A_1 to accurately amplify the noise sampled at the summing node. The time constant associated with the settling at the output of A_1 is determined by its output resistance, $R_{\rm OUT1}$, and capacitor C_2. For complete noise cancellation, the time allowed for settling, $T_{\rm DEL}$ in Fig. 9(b), must be much longer than the settling time constant. The residual noise due to incomplete

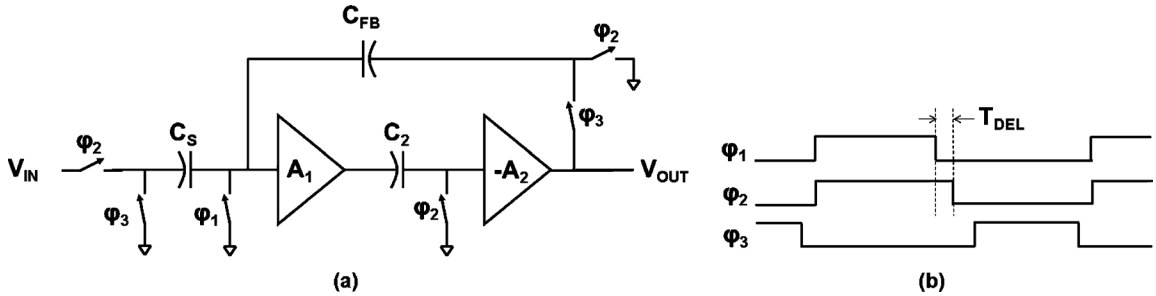

Fig. 9. Active noise cancellation of sampled noise. (a) Configured as a track-and-hold amplifier. (b) Switch control timing diagram.

settling can be modeled as the exponential decay of a single pole system

$$\overline{\mathrm{v}_{\mathrm{n,sample}}^2} = \frac{\mathrm{kT}}{\mathrm{C_S}}\left(\frac{\mathrm{C_S}+\mathrm{C_{FB}}+\mathrm{C_P}}{\mathrm{C_S}}\right)\left(\exp^{-\frac{\mathrm{T_{DEL}}}{\mathrm{R_{OUT1}C_S}}}\right). \tag{14}$$

During the time between the falling edges of φ_1 and φ_2, the input voltage is still connected to the input of A_1 through the sampling capacitor. Any change in the input voltage is amplified at the output of A_1. Because this amplified version of the input is sampled on C_2, it is important that the amplified signal be linear in order to avoid distortion in the φ_3 output. The requirement for linearity demonstrates why, while it is best for noise, a very large A_1 is not necessarily an optimal design trade-off.

In order to quantify the impact of A_1, the required input bandwidth must be defined. For an input sinusoid of amplitude V_{ampl} at a maximum input frequency f_{max}, the maximum voltage change at the output of amplifier A_1 is

$$\Delta \mathrm{v_{max}} = \mathrm{A_1 V_{ampl} 2\pi f_{max} T_{DEL}}. \tag{15}$$

This voltage change Δv_{max} must be within the linear signal swing of the amplifier. Therefore, as T_{DEL} is increased in order to reduce noise from the C_S sample, or as the gain of A_1 is increased in order to reduce noise from the C_2 sample, the output swing requirements of A_1 are increased. The output swing requirement is also directly related to the input signal bandwidth. Finally, A_1 must be capable of providing transient current to C_2, a requirement that scales with input signal frequency and the value of capacitor C_2.

For relatively slow moving input signals, the proposed noise cancellation technique can be particularly powerful. By using a long T_{DEL} and large C_2, the total sample phase noise can be extremely small, regardless of the sampling capacitor size. This can be advantageous in the case of oversampled systems; a small input capacitance is easy to drive during a short track time, while the comparatively slow moving input allows for significant noise reduction without placing difficult requirements on A_1.

C. Prototype Implementation

In order to verify the active noise cancellation technique, the circuit shown in Fig. 9(a) has been implemented and embedded in a signal chain similar to Fig. 6(b). This test chip #2 is fabricated in a 65 nm CMOS process. The ADC clock rate is 20 MSPS. The size of the sampling capacitor is 2.3 pF. Other than the sampling capacitor, capacitance at the summing node totals 2.4 pF. The time constant at the output of amplifier A_1 is 550 ps. Based on calculation, the kT/$\mathrm{C_S}$-limited sampled thermal noise should be 84 μV-rms. Note that this calculation only includes the noise at the summing node and represents a lower limit to the achievable total sample phase noise; if offset cancellation were required and the impact of auto-zero capacitor C_2 were included in the calculation, the sample phase noise would be higher.

In consideration of the power dissipation of this test chip, there is effectively no impact due to the use of noise cancellation. The first stage amplifier design is constrained primarily by the need to maintain stable closed loop operation during phase φ_3. Given this amplifier design, the noise cancellation technique works well for $T_{\mathrm{DEL}} \sim 1$ ns. As predicted by (15), the amplifier output swing requirement is reasonable for inputs at the Nyquist frequency of 10 MHz. However, to support significantly higher input frequencies, the first stage amplifier power dissipation would be increased.

Fig. 10 shows data measured from test chip #2 as time T_{DEL} is swept. The two solid lines shown correspond to configurations varying the size of auxiliary capacitor C_2. With $T_{\mathrm{DEL}} = 0.1$ ns, there is very little cancellation of noise, as amplifier A_1 does not have adequate time to respond to the thermal noise sampled at the summing node. The maximum noise, $\sim$100 μV-rms, is larger than kT/C_S due to the additional noise contributed by the C_2 sample. As expected, as T_{DEL} is increased, the measured noise decreases. Most of the noise cancellation benefit is achieved for T_{DEL} equal to roughly two time constants, a result that can be predicted by (14).

Fig. 10 also compares the measured results to the prediction of a simple model, shown by dotted lines. The model is based on (14) as well as calculations to refer noise sampled on C_2 to the input. For T_{DEL} less than 0.55 ns, the model prediction matches the measured results to within 5%. For longer T_{DEL}, there is a more significant discrepancy between the measured data and the model prediction. One possible explanation is that the noise sampled on C_S is not completely cancelled. An alternative explanation is the presence of a noise source that is present in the prototype measurement but not accounted for in the model. The magnitude of this unmodeled noise source would be roughly 32 μV-rms, referred to the summing node. Unfortunately, test modes in silicon were not adequate to diagnose the root cause.

With regards to the overall sample phase noise power, test chip #2 demonstrates a reduction of 67% or 4.8 dB, from 96 μV-rms to 55 μV-rms. Considering only the thermal noise

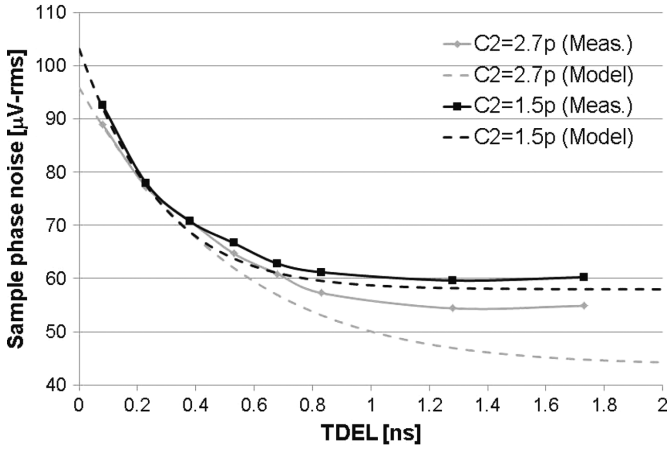

Fig. 10. Measured sample phase noise on test chip #2 versus settling time, with varying size of auxiliary capacitor C_2.

power sampled at the summing node, it is effectively cancelled by at least 85%, from 84 μV-rms to 32 μV-rms. It is relevant to note the significant cancellation of noise sampled at the summing node, as the additional noise from the second sample at the output of A_1 may be reduced much further for applications in which the input signal bandwidth is limited.

V. Conclusion

While it has been commonly accepted as a fundamental limit of thermal noise when sampling on a capacitor, kT/C is, in fact, not a limit at all. This paper presented two circuit-level sampling techniques that allow the size of the input capacitor to be determined almost independently of the noise requirement. The first method broke the relationship between the sampling bandwidth and the dominant noise source. The second technique used active circuits and a second capacitor not driven by the input to cancel the noise sampled on the input capacitor. Test chip measurements were presented to demonstrate that the effective sampled thermal noise can be reduced by as much as 67% without change to the input capacitor. These techniques provide a powerful new degree of freedom in design, making possible circuits that are both low noise and easy to drive.

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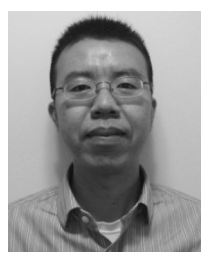

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