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An efficient design of full adder in quantum-dot cellular automata (QCA) technology

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ABSTRACT

The full adder circuit is a basic unit in digital arithmetic and logic circuits. In this paper an improved full adder in QCA technology is proposed. This design is considerably declined in terms of cell numbers and area, compared to other full adders and delay is kept at minimum. To design this full adder a different formulation for sum and carry outputs of full adder has been used. The simulation results in QCADesigner software confirm that the presented circuit works well and can be used as a high performance design in QCA technology. Finally, the proposed QCA full adder is used to make three sizes of ripple carry adders (RCA) and acceptable results are achieved.

1. Introduction

In the near future, it is expected that the CMOS technology reaches to the end of its roadmap because of many serious challenges such as short channel effect, impurity variations, high cost of lithography and more importantly, the heat [1–3]. So, many technologies such as Single Electron Transistor (SET), Resonant Tunneling Diode (RTD), Carbon Nanotube Field Effect Transistor (CNFET) and Quantum dot Cellular Automata (QCA) have been emerged to solve the mentioned problems [3–5]. According to the international technology roadmap for semiconductors (ITRS) report which offers an accurate summary of future technologies, QCA is one of the promising future solutions [6].

The QCA is a powerful alternative to use in VLSI circuits because of its ability to achieve high performance in terms of device density, clock frequency and power consumption [4,7,8]. This technology is based on a specific physical phenomenon, called Coulomb repulsion, which uses location of electron pairs instead of voltage levels for logical modes. The data is represented by cells polarizations, which are controlled by inputs and clock signals [7,9]. A key advantage of QCA devices is the simplified interconnection which is possible with this paradigm. Since the cells communicate only with their nearest neighbors, there is no need for long interconnection lines. The inputs are applied to the cells at the edge of the system and the computation proceeds until the output appears at cells at the edge of the QCA array [10].

Physical and algorithmic based designs are two different aspects which are studied in QCA. In high level designs, concentration is on the logical and algorithmic design as well as the physical design. However, physical interactions can be disruptive in device performance. Therefore, control of the physical interactions is a necessary problem in the real QCA circuit designs, especially in large systems [11].

The circuits in QCA technology have been designed and improved in the terms of area, complexity, and delay. Many logical devices such as memory [12,13], adders [5,14–20] and sequential circuits [21–27] are implemented in QCA technology. The fabricatable layout designs of QCA are also proposed in [26–28].

This paper introduces a new QCA full adder design using a different formula for sum which is enhanced in term of cell numbers in comparison to other approaches proposed in the literature. Using this approach provides improved area and delay to other recent designs. For evaluating the proposed QCA full adder in larger adders, we have designed the ripple carry adders (RCA) using the proposed full adder in sizes of 4-bit, 8-bit and 16-bit which have significant features.

This paper is organized as follows. A brief background of QCA architecture is studied in Section 2. We have reviewed previous presented circuits of one-bit full adders and their QCA layouts in Section 3. Section 4 is introduced our proposed one-bit full adder

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circuit and its new formulation for sum is proved. In Section 5, the layout of proposed QCA full adder and the simulation results are described and a comparison has been done between the proposed full adder and some recent implementations for evaluation. Finally, we have concluded this paper in Section 6.

2. Architecture of QCA

In this part, some basic concepts of QCA technology including logic gates, interconnections and clocking are described.

2.1. QCA cell

The QCA cell is a square structure in nano-scale that consists of four quantum dots and two electrons. The electrons are able to tunnel between quantum dots if the potential barrier that separates quantum dots is low. According to Coulomb repulsion, electrons occupy two opposite corners of the cell. Consequently, the four quantum dots in each QCA cell can be in two stable polarization states. These states can be used to encode binary information. Two configurations for the cells can be created by occupation of corner dots as shown in Fig. 1. The −1 and 1 polarizations are equal to binary values zero and one, respectively [9]. In QCA technology, switching is succeeded by switching the occupancy of the two electrons [19].

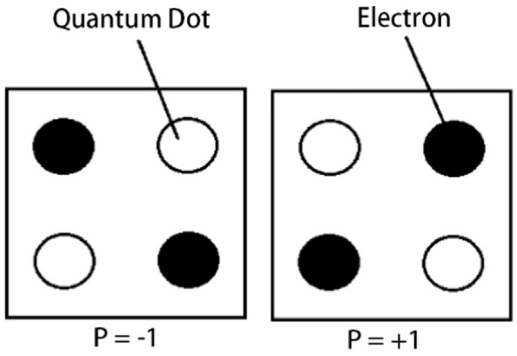

Fig. 1. QCA cell.

2.2. Logic gates

The topology of the QCA layout defines the interaction of the cells and hence the functionality of the overall circuit [19]. All conventional logic gates can be constructed using QCA cells. The majority gate is the basic block of QCA circuits. Fig. 2 (a) demonstrates the structure of the majority gate that consists of three input cells, one inside cell and one output cell.

The tendency of the inside cell is moving to a ground and consequently it gets the polarization of the majority of its neighbors. The inside cell will tend to follow the majority polarization since it represents the lowest energy state [5].

An AND gate or OR gate will be obtained by fixing the polarization of one input to the majority gate as logic 1 or logic 0. As demonstrated in Table 1, if one input is set to 0, the majority gate gives the AND of the two other inputs. Also, if one input is set to 1, the majority gate gives the OR of the two other inputs. We can use the advantage of this property in design of circuits.

The other structure block is the inverter gate which has different layouts in QCA designs. The schematic and different layouts of the inverter gate are shown in Fig. 2(b). According to the Coulomb repulsion, the lowest energy state for two diagonally adjacent cells is when they have opposite polarities.

The QCA designers can implement all logical functions with a combination of majority gates and inverter gates [5].

2.3. QCA circuit internal connections

Input data is carried down arrays of QCA cells due to interaction of adjacent cells. Binary data is transmitted from one physical location to another location by a wire. Once the polarization of a

Table 1
Truth table of majority gate.

A	B	C	M(A, B, C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

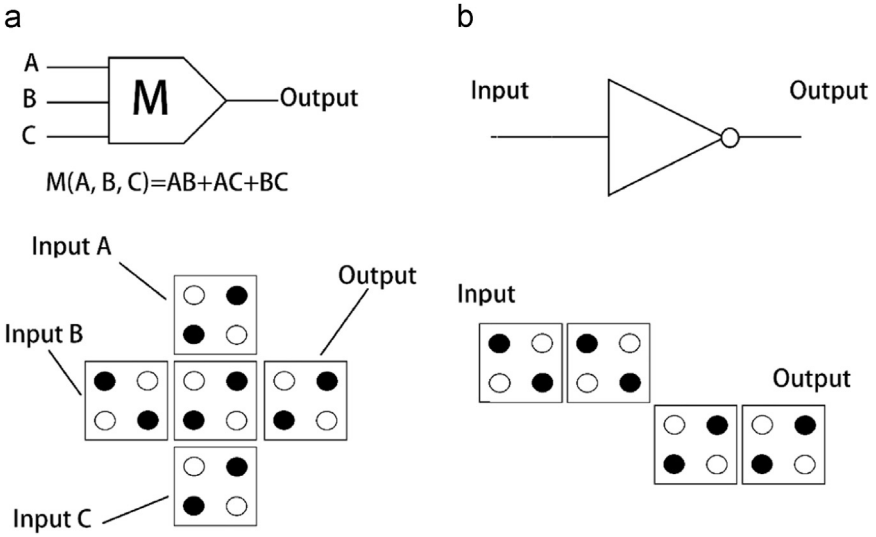

Fig. 2. Structure blocks of (a) majority gate and (b) inverter gate.

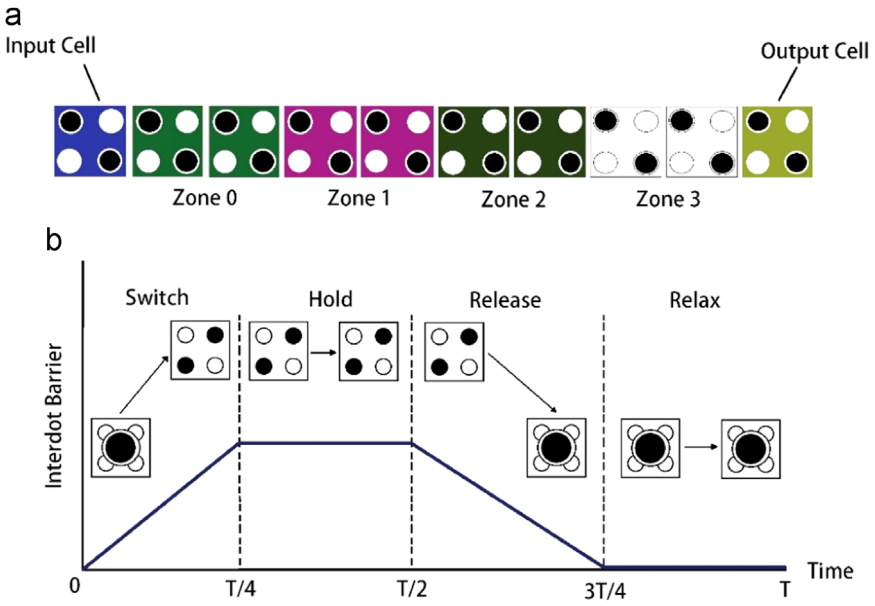

Fig. 3. Diagram of (a) a wire and its clock zones and (b) switching between four phases of a clock.

QCA cell is fixed, the encoded binary information is transferred to adjacent cells. A wire as shown in Fig. 3(a) includes an input cell and a number of free cells. Coulomb interaction causes a value of logical zero or one from input be published through the chain of the free cells [5].

For arrangement of the circuit timing, namely when the input values reach to the target places, the signal clocking is used. Such as the entrances of the majority gate that the values must reach at the same time into them. In the signal clocking, QCA cells are divided to four time zones. Each time zone, also called clock zone, corresponds to one of the four phases: switch, hold, release and relax (Fig. 3(b)). During the switch phase, interdot potential barriers are lowered and data propagation occurs via electron tunneling. By gradually raising the barriers, the cells become polarized. For the hold phase the barriers are held high so the cell maintains the polarization and the output can be used as inputs to the next stage. During the release and relax phases, the QCA cells start to lose their polarization by lowering the barriers and then they remain in an unpolarized state.

The power consumption of QCA is low since only two electrons are moving. Most of the power required by QCA circuits will be used by the clocking scheme [19].

2.4. Crossover multi-layer

Fig. 4 indicates the structure of multi-layer crossover. As QCA regular cells (not 45 degrees cells) are used in this paper, multi-layer crossovers are utilized in this design. According to Coulomb repulsion, the polarization of stacked cells becomes inverse when the value is passing between layers. Therefore, the multi-layer crossover requires at least three layers for implementation.

3. One bit QCA full adder designs

In this section, we review various schematic formulations of one-bit full adders and their QCA layouts which have been presented in other papers. In the all following adders, A, B and C are binary inputs and sum and carry represent the outputs. The first one which was presented in 1994, shown in Fig. 5(a), consists of five majority gates and three inverters [7]. The QCA layout of this design uses 192 cells and implemented in one layer. In this design

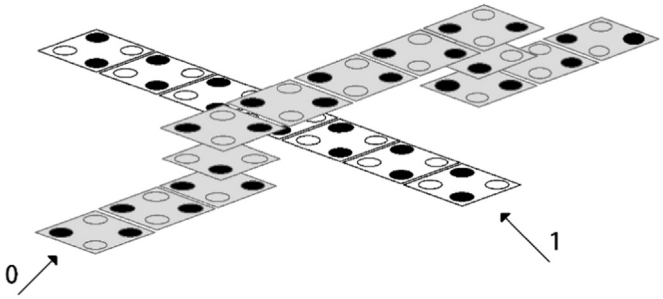

Fig. 4. Structure of multi-layer crossover.

QCA clocking concepts are not considered [7]. A modification of this design is shown in Fig. 5(b) which has four majority gates and three inverters [16].

Another design of QCA full adder has three majority gates and two inverters as shown in Fig. 6(a) [5]. The QCA layout of this design has five clocking phases and uses 145 cells [5].

A distinct design of full adder was presented in [29]. As shown in Fig. 6(b), this design employs a three-input majority gate, one inverter, and an unconventional form of majority gate with five inputs. A QCA layout for this design was proposed in 2012 that has three clocks and uses only 51 cells [14]. A modified form of this design has two inverters at the entrance of five inputs majority gate instead of one inverter that was presented in 2010. The QCA layout of this design has three clock phases and uses 73 cells [16].

As demonstrated in Fig. 7, another design of full adder consists of three majority gates and two inverters [30]. The QCA layouts of this design has three clock phases and also has 82 cells in type-1 and 86 cells in type-2 [30].

4. Proposed QCA full adder

To design our improved full adder, we need a new formulation for sum output of full adder. In a full adder, carry and sum are defined as Eqs. (1) and (2).

$$\text{Carry} = ab + bc + ac = M(a, b, c) \tag{1}$$

$$\text{Sum} = abc + \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} \tag{2}$$

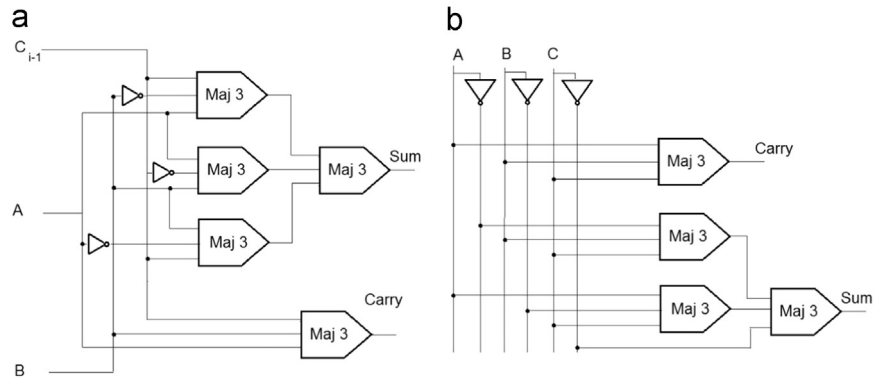

Fig. 5. (a) One bit QCA full adder presented in [7] and (b) modified design of previous one bit QCA full adder [16].

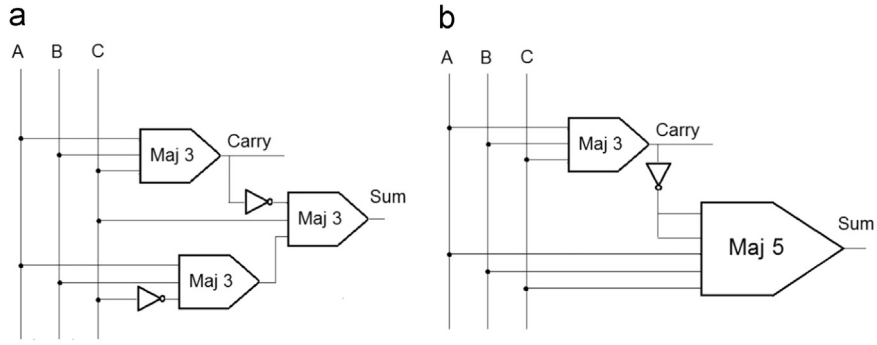

Fig. 6. (a) One bit QCA full adder presented in [5], and (b) one bit QCA full adder presented in [29].

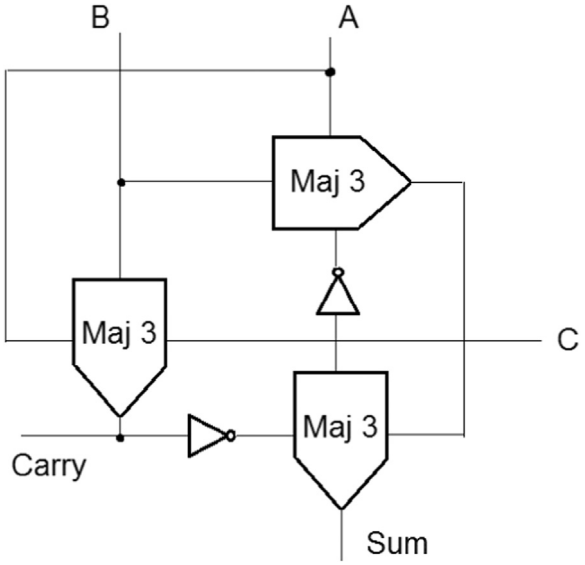

Fig. 7. One bit QCA full adder presented in [30].

In above equations, M represents the majority gate. The carry output is generated by a majority gate. Since the majority gate is the basic gate in QCA technology, carry output is optimum. We have to minimize the sum equation in terms of the majority gates. We can show that the sum output can be generated by Eqs. (3)–(5).

$$= \mathrm{M}\left(\overline{\mathrm{Carry}}, \mathrm{M}\left(\mathrm{a}, \mathrm{b}, \overline{\mathrm{Carry}}\right), \mathrm{c}\right) \tag{3}$$

or

$$= \mathrm{M}\left(\overline{\mathrm{Carry}}, \mathrm{M}\left(\mathrm{a}, \mathrm{c}, \overline{\mathrm{Carry}}\right), \mathrm{b}\right) \tag{4}$$

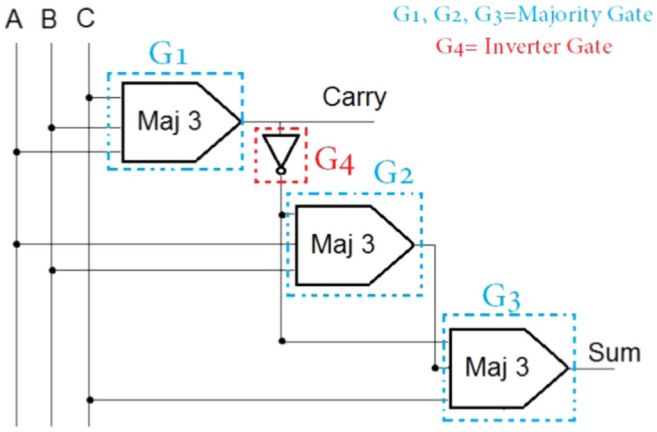

Fig. 8. The schematic of proposed full adder.

or

$$= \mathrm{M}\left(\overline{\mathrm{Carry}}, \mathrm{M}\left(\mathrm{b}, \mathrm{c}, \overline{\mathrm{Carry}}\right), \mathrm{a}\right) \tag{5}$$

Eq. (3) is proved as follows and Eqs. (4) and (5) can be proved similarly.

$$\mathrm{M}\left(\overline{\mathrm{Carry}}, \mathrm{M}\left(\mathrm{a}, \mathrm{b}, \overline{\mathrm{Carry}}\right), \mathrm{c}\right) = \mathrm{M}\left(\overline{\mathrm{M(a,b,c)}}, \mathrm{M}\left(\mathrm{a}, \mathrm{b}, \overline{\mathrm{M(a,b,c)}}\right), \mathrm{c}\right)$$

$$= \mathrm{M}\left(\left(\mathrm{a}\overline{\mathrm{b}} + \overline{\mathrm{a}}\,\overline{\mathrm{c}} + \mathrm{b}\overline{\mathrm{c}}\right), \mathrm{M}\left(\mathrm{a}, \mathrm{b}, \left(\mathrm{a}\overline{\mathrm{b}} + \overline{\mathrm{a}}\,\overline{\mathrm{c}} + \mathrm{b}\overline{\mathrm{c}}\right)\right), \mathrm{c}\right)$$

$$= \mathrm{M}\left(\left(\mathrm{a}\overline{\mathrm{b}} + \overline{\mathrm{a}}\,\overline{\mathrm{c}} + \mathrm{b}\overline{\mathrm{c}}\right), \left(\mathrm{ab} + \overline{\mathrm{a}}\mathrm{b}\overline{\mathrm{c}} + \mathrm{a}\overline{\mathrm{b}}\overline{\mathrm{c}}\right), \mathrm{c}\right)$$

$$= \mathrm{abc} + \overline{\mathrm{a}}\mathrm{b}\overline{\mathrm{c}} + \overline{\mathrm{a}}\mathrm{b}\overline{\mathrm{c}} + \mathrm{a}\overline{\mathrm{b}}\overline{\mathrm{c}} = \mathrm{Sum}$$

Fig. 8 which shows the schematic of Eq. (3), uses three majority gates and one inverter. Though, it seems not to be a significant

improvement respect to the design in Fig. 7, the QCA layout of our design is considerably simpler than the one in Fig. 7. In the next section we show the layout of the proposed circuit which designed in QCADesigner.

4.1. One-bit QCA full adder design

As is shown in Fig. 9, the layout of the proposed circuit has only 38 cells and it needs three clock phases to generate the sum and carry outputs. The proposed QCA full adder uses conventional QCA cells and is implemented in three layers.

Fig. 10 demonstrates three layers of the proposed QCA full adder separately. A, B and C represent input cells while carry and sum are output cells. Parts of G1, G2 and G3 display the majority gates and part of G4 shows the inverter gate in layer 1. There are two cells in layer 2 that link layer 1 to layer 3. Layer 3 makes a connection between two areas of layer 1 via layer 2.

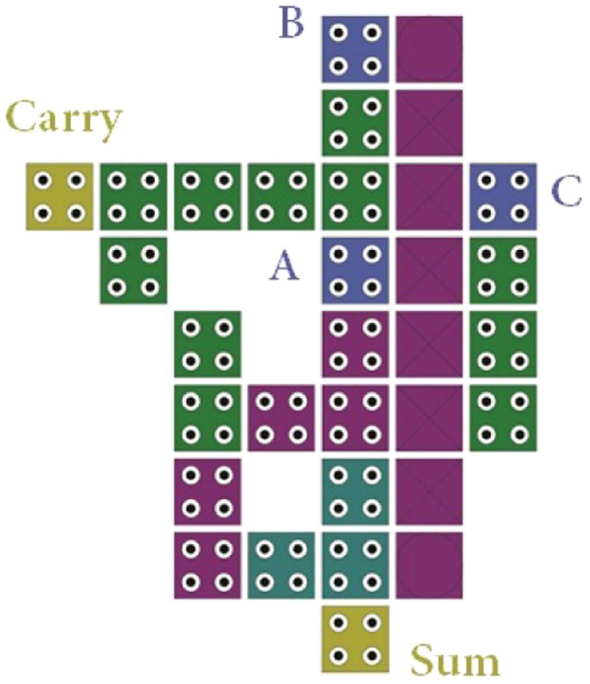

Fig. 9. Layout of the proposed QCA full-adder in three layers.

4.2. Ripple carry adder (RCA) design

The proposed QCA full adder is implemented in three layers which needs to a little modification for larger adders such as ripple carry adder. We used some cells to move the place of input A in the main layer as shown in Fig. 11.

For these designs, two new layers are added below the main layer to transmit the value of input A into the first majority gate. Therefore, we implement the ripple carry adders in five layers including: sub-layer, via −1, main layer, via 1, crossover layer.

The sub-layer, which is the lowest layer, includes only the cells of input A as a wire relating to the input A transmition value. There are two cells for each input A to connect the main layer and the sub-layer in via −1, which is placed between the main layer and the sub-layer.

All input and output places are positioned in the main layer. The cells in via 1 and crossover layers are same as the proposed full adder. Different layers of the modified proposed full adder are demonstrated in Fig. 12.

The ripple carry adder layout in size of 4-bit is indicated in Fig. 13. This design uses 237 cells in its structure which requires 6 clock phases to genereate the final output. In this implemention, 12 convential majority gates are used.

The layout of ripple carry adder in size of 8-bit is shown in Fig. 14. It is composed of 517 cells and the output is generated after 10 clock phases. This design is made of 24 the three-input majority gates.

Fig. 15 demonstrates the layout of ripple carry adder in size of 16-bit. This implemention consists of 1224 cells which needs 18 clock phases for generating the correct output. This design is made up of 48 convential majority gates.

5. Simulation and experimental results

In this part, we simulate the proposed QCA full adder and the ripple carry adders (RCA) using the proposed full adder in sizes of 4-bit, 8-bit and 16-bit by QCADesigner version 2.0.3 tool [31,32].

All parameters and conditions of this simulation are default values in QCADesigner as follows. The size of the basic quantum cell was set at 18 by 18 with 5 nm diameter quantum dots. The center-to-center distance was set at 20 nm for adjacent cells. The following parameters are used for a bistable approximation: 0.001 convergence tolerance, 65 nm radius effect, 12.9 relative

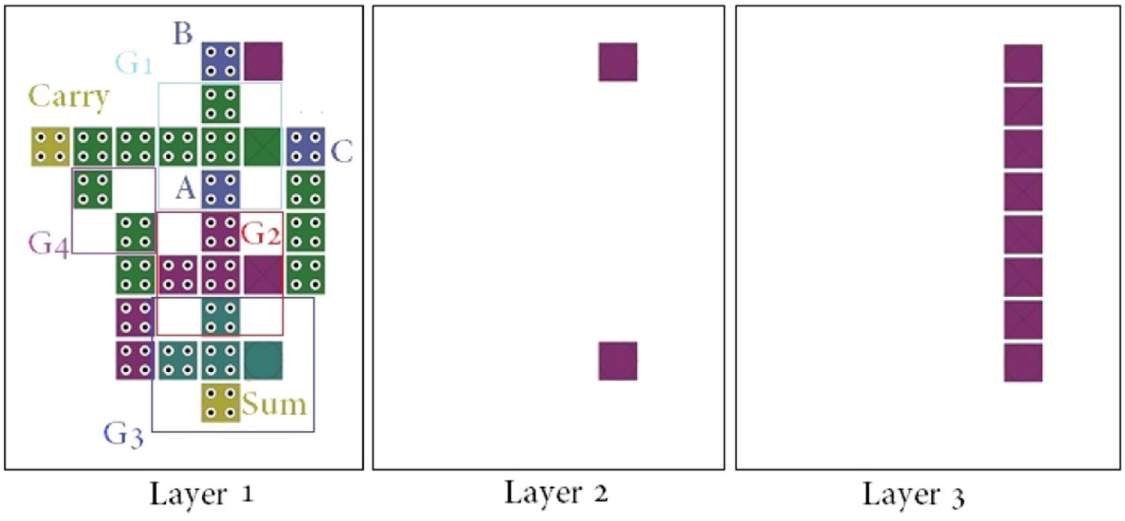

Fig. 10. Three different layers of the proposed QCA full-adder.

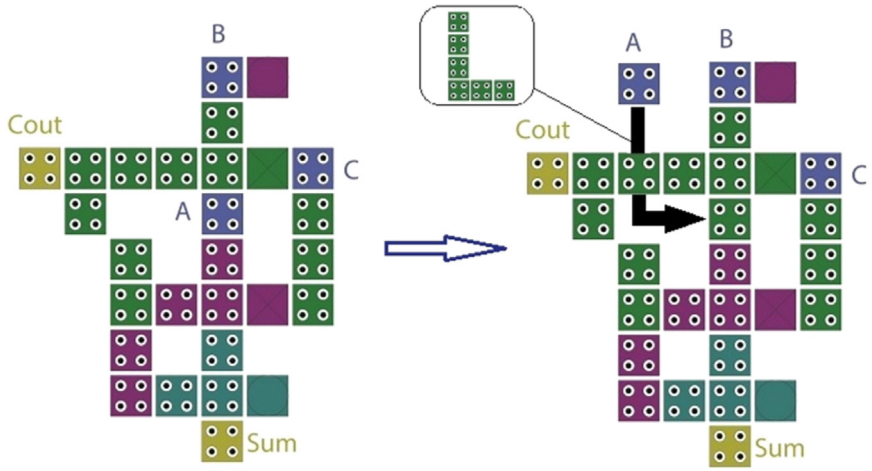

Fig. 11. Modification of the input A place.

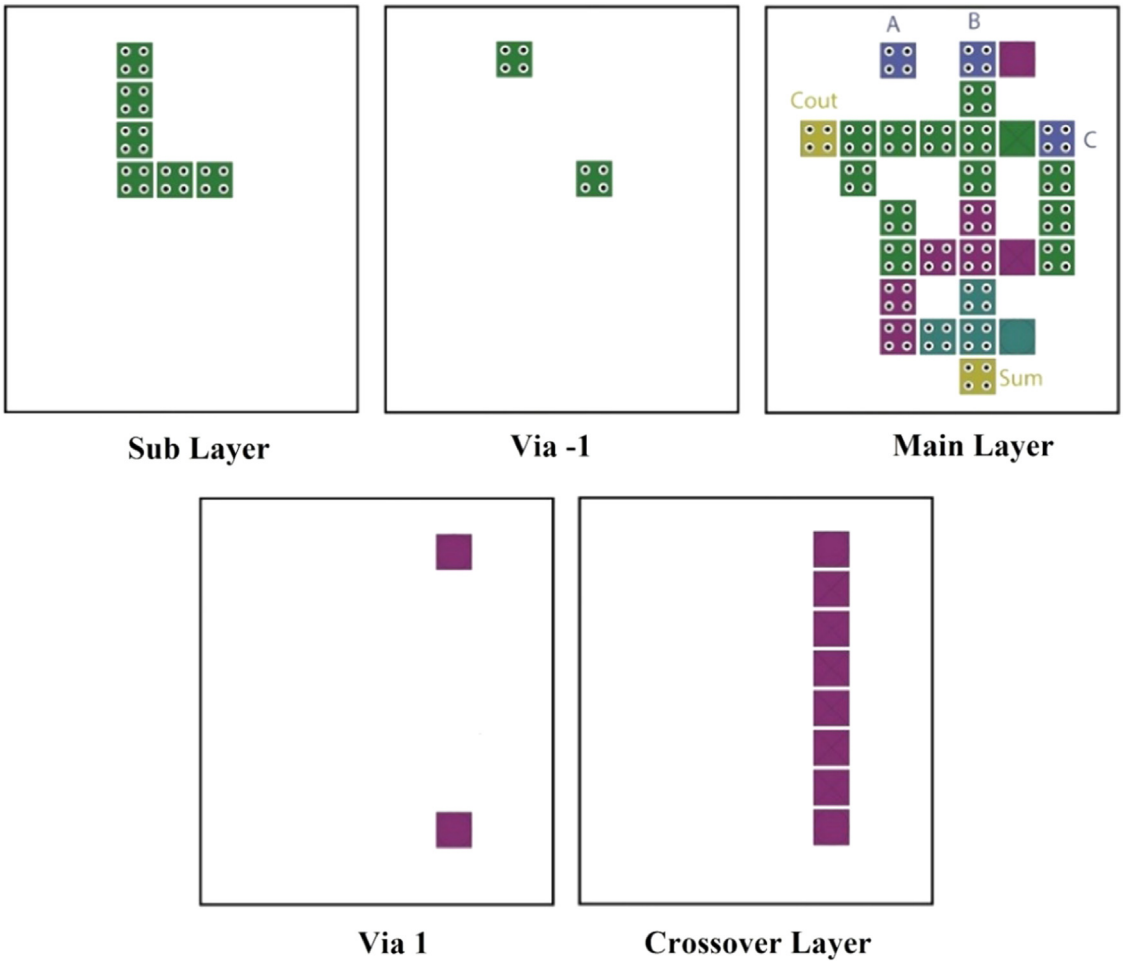

Fig. 12. Different layers of modified proposed full adder.

permittivity, 9.8e−22 clock high, 3.8e−23 clock low, 1 clock amplitude factor, 11.5 layer separation, and 100 maximum iterations per sample.

5.1. Simulation of the proposed QCA full adder

The results of simulation for all combinations of A, B, and C inputs are shown in Fig. 16. Simulation results confirm that the proposed QCA full adder works well and indicate appropriate performance. As an instance, for inputs of A=0, B=1 and C=0, the correct outputs of carry=0 and sum=1 are generated as demonstrated in Fig. 16.

A comparison between the proposed QCA full adder and all the full adder designs discussed in this paper is accomplished in order to evaluate the features of proposed full adder. Also, the layouts presented in [11,33–35] are contributed in the comparison. Table 2 confirms that the cell numbers and area of the proposed full adder have improved as delay kept at the lowest level.

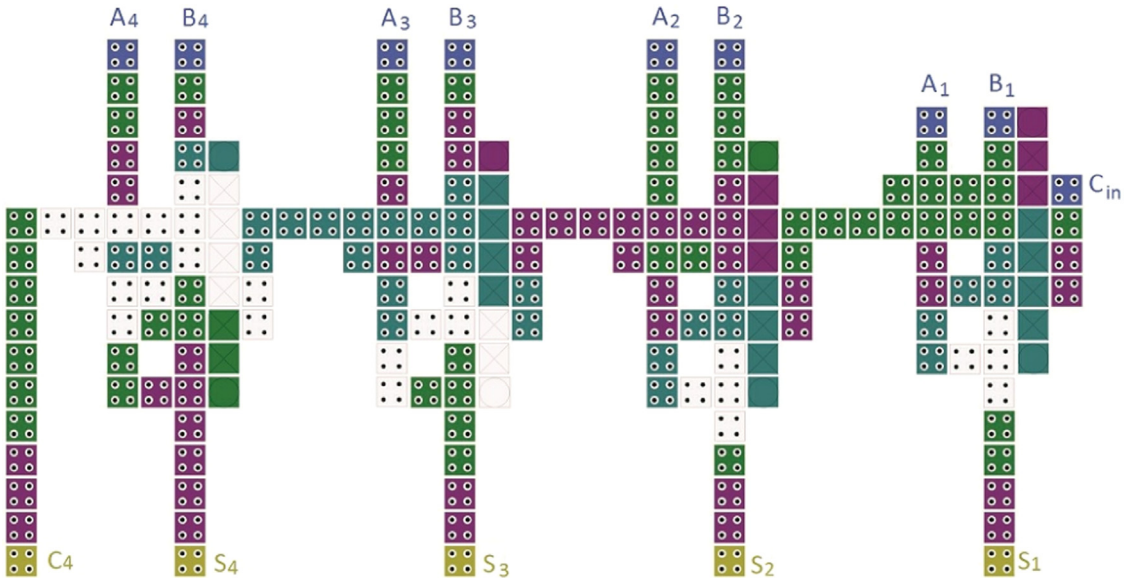

Fig. 13. The layout of 4-bit ripple carry adder.

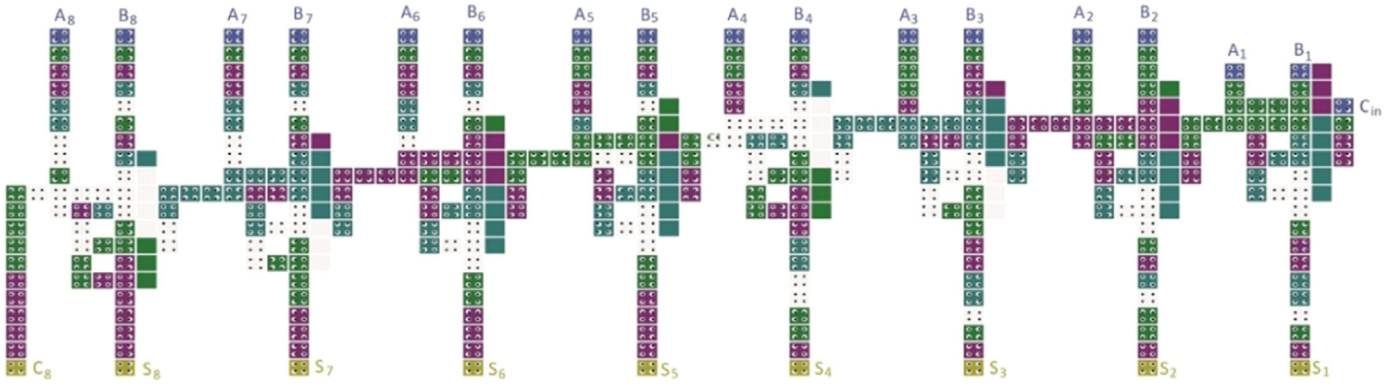

Fig. 14. The layout of 8-bit ripple carry adder.

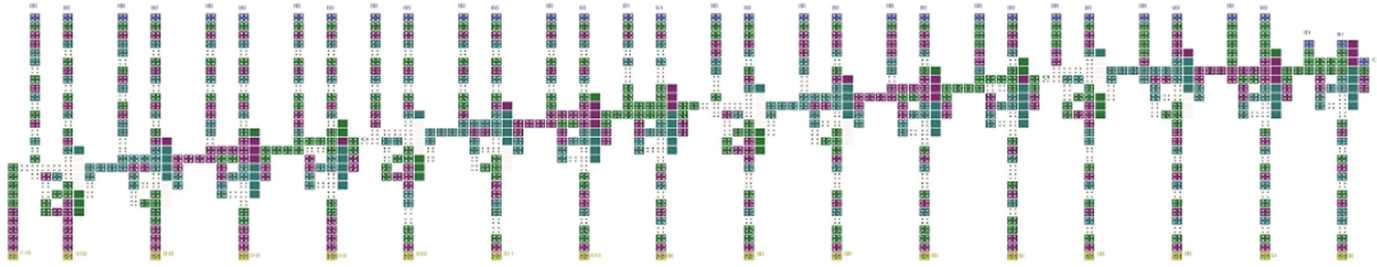

Fig. 15. The layout of 16-bit ripple carry adder.

5.2. Simulation of the ripple carry adders (RCA)

The features of the proposed ripple carry adders (RCA) in sizes of 4-bit, 8-bit and 16-bit are shown in Table 3.

To evaluate the features of the ripple carry adders, a comparison is made between these designs and the designs presented in [11,14] and [35]. Table 4 shows the features of ripple carry adders (RCA) presented in the mentiond designs.

According to Tables 3 and 4, the proposed ripple carry adders have acceptable features in the terms of cell numbers, area and delay. The proposed RCA uses 64% and 33% in size of 4-bit, 65% and 25% in size of 8-bit, 67% and 30% in size of 16-bit less cells in comoparison to [11] and [14], respectively.

The proposed RCAs occupy less area than the designs in [11] and [14] in all the sizes. Moreover, the proposed RCAs need less delay than the designs in [11] and [14].

6. Conclusion

In this paper, an optimized full adder in QCA technology is presented. The proposed full adder was enhanced in terms af area,

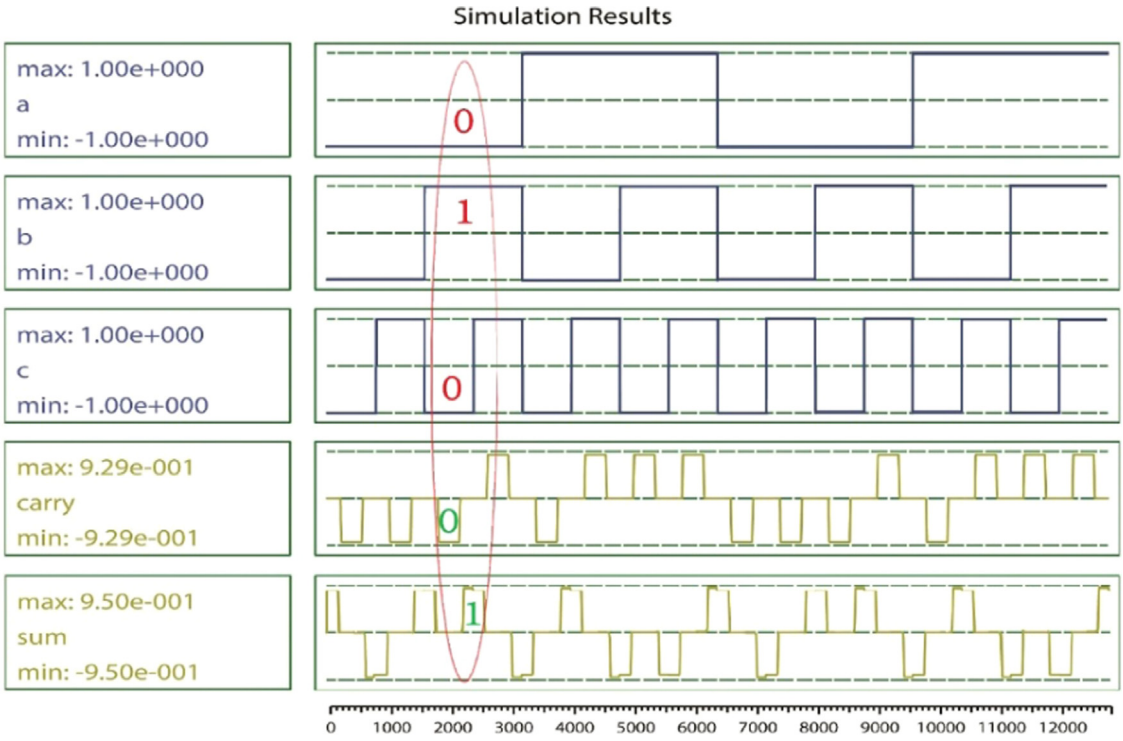

Fig. 16. Simulation of the proposed QCA full adder.

Table 2
Comparison of QCA full adders.

	Number of cells	Area (μm^2)	Delay (clock phases)
[7]	192	0.20	Not applicable
[19]	292	0.62	14
[5]	145	0.17	5
[11]	135	0.14	5
[35]	102	0.10	8
[30,36]	86	0.10	3
[36]	82	0.03	3
[16]	73	0.04	3
[33]	69	0.07	4
[34]	61	0.03	3
[14]	51	0.03	3
Proposed design	38	0.02	3

Table 3
The features of the proposed ripple carry adders (RCA).

	Number of cells	Area (μm^2)	Delay (clock phases)
RCA 4-bit	237	0.24	6
RCA 8-bit	517	0.59	10
RCA 16-bit	1224	1.55	18

Table 4
The features of ripple carry adders (RCA) presented in [11,14] and [35].

		Number of cells	Area (μm^2)	Delay (clock phases)
RCA 4-bit	[11]	651	1.20	17
	[14]	308	0.29	8
	[35]	558	0.85	20
RCA 8-bit	[11]	1499	3.56	33
	[14]	695	0.79	15
	[35]	1528	2.93	36
RCA 16-bit	[11]	3771	11.77	65
	[14]	1759	2.51	20
	[35]	4652	10.85	68

complexity and delay. In the proposed design, we used a new formulation of full adder outputs. In addition of an efficient formulation, arrangement of QCA cells is also important to achieve an efficient and high performance implementation. Table 2 sumurizes three important parameters of various designs of full adders proposed in previous works and this paper. As is shown, our design uses 38 QCA cells whereas two good designs peoposed in [16] and [14], use 73 and 51 QCA cells which means 50 and 26 percent improvements, respectively. Area of the layout is also reduced in our proposed circuit. The delay, defined as the clock phases needing to transfer the input signals to the output, is three for three last circuits which is minimum.

To evaluate the proposed QCA full adder in larger adders, we designed the ripple carry adders (RCA) using the proposed full adder in sizes of 4-bit, 8-bit and 16 bit which had acceptable features (Table 3). A comparison between the proposed RCAs and good RCA designs proposed in [11] and [14] showed that our proposed RCAs have better performance.

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