Load Commutated SCR based Current Source Inverter fed Induction Motor Drive with Open-end Stator Windings

Richu Sebastian C and P.P.Rajeevan

***Abstract*—A new topology of load commutated SCR based current source inverter fed induction motor drive with open-end stator winding is presented in this paper. The proposed topology has a current source inverter (CSI) at one side of the stator winding and a capacitor fed voltage source inverter (VSI) at the other end. The CSI feeds only active power to the motor and the VSI is controlled to provide the reactive power required for operation of the CSI at leading power factor thereby facilitating natural commutation of SCRs. This topology does not require any interfacing inductor or separate DC voltage source for the VSI. The control scheme enables operation of the motor even at very low speeds without problems like commutation failure. The experimental verification of the proposed scheme is carried out on an induction motor with open-end stator windings. A digital signal processor (TMS320F28335) is used for implementation of the control algorithm.**

***Index Terms*— Motor drives, induction motor drives, inverters.**

I. INTRODUCTION

Current source inverters (CSI) are preferred in many high power drive applications due to certain advantages compared to the voltage source inverters (VSI), even though the latter is commonly used in many of the low and medium power applications[1]-[4]. Since the CSI is fed from a well regulated current source with a large inductor it has inherent short circuit protection. It is also free from problems like DC bus shoot through fault, encountered in VSI. These features enhance the reliability and ruggedness of the CSI fed drive systems [4].Another feature of the CSI fed drive which makes it a preferred choice in many high power applications is its inherent regenerative capability. The main drawback of CSI fed drive is that since large inductors are used for realizing the current source, they have slower dynamic response compared to that of VSI fed drives. However most of the medium and high power drives are used for loads like pumps, fans, conveyers and compressors where high dynamic performance is not a requirement. CSI fed drives are ideally suited for such high power applications [1].

Silicon Controlled Rectifier (SCR) is one of the most rugged power semiconductor devices, available in high current and voltage ratings. Since the SCRs can block both forward and reverse voltages in the OFF state they are well suited for current source inverters. However, being a semi-controlled device an SCR can only be turned ON by applying gate pulse but turning OFF (commutation) requires its anode current to be brought down below the holding current. Hence complex forced commutation circuits are required for SCRs, in many applications. In AC circuits, natural commutation of the SCR can be achieved if the current through the device is leading ahead of the voltage. In other words, SCRs can be naturally commutated if they are used in CSI feeding loads that operate at leading power factor. A synchronous motor can be operated at leading power factor by resorting to over-excitation thereby making the motor current leading ahead of the voltage. This feature makes the SCR an ideal switching device in the CSI fed synchronous motor drive since the SCRs will be naturally commutated by the motor (load commutation) during the inverter operation [4]. SCR based load commutated CSI fed synchronous motors are extensively used in high power drive applications [3]. When compared to synchronous motors, the induction motors are more rugged, reliable, cheaper, and efficient and hence always preferred in industrial applications. The simple rotor structure and the absence of any moving contacts make a squirrel cage induction motor almost maintenance-free. However, since the induction motor operates at lagging power factor it was not possible to achieve load commutation of SCRs in CSI fed induction motor drives unlike synchronous motor drives. Hence gate turn-off thyristor (GTO) based CSI was developed for induction motor drives [5],[6]. However the complexity of the gate drive circuit and the requirement of high negative current pulses (20-25% of the anode current) for turn OFF, limited the use of GTOs in CSI, especially for high power applications [1]. If the load commutation can be achieved in SCR based CSI fed induction

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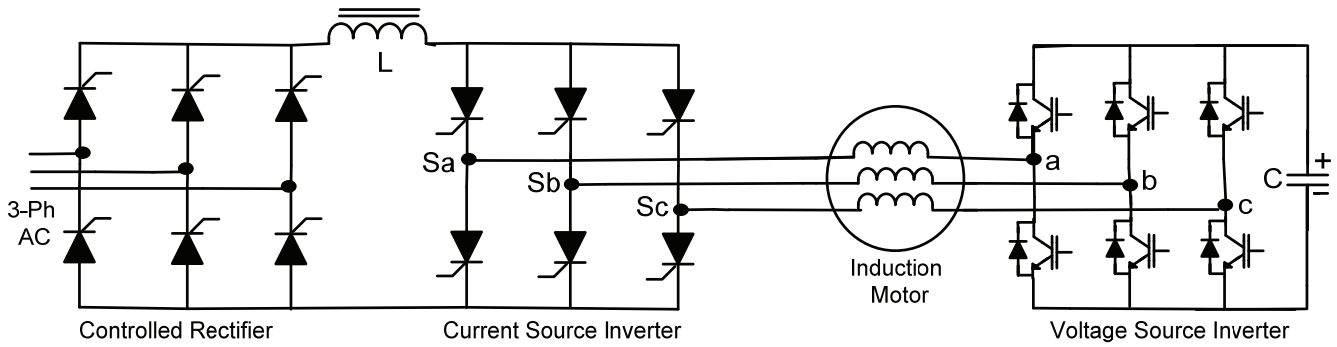

Fig.1 The proposed load commutated CSI fed induction motor drive with open-end stator windings

motor drive, it would be a very good choice in many high power drive applications. Hence many researchers in this field were trying to develop schemes to achieve load commutation in SCR based CSI fed induction motor drives.

Induction motor drive with parallel AC power capacitors at the motor terminals was one of the schemes tried for achieving load commutation, initially [1],[7],[8]. A major drawback of this scheme was the resonance between the parallel capacitor bank and the motor inductance, in addition to the commutation failure at slow speeds due to insufficient reactive power compensation. Hence external commutation circuit is required in this scheme for low speed operation and starting [1],[7]. Later many hybrid topologies comprising of SCR based CSI and VSI connected in parallel at the induction motor terminal were proposed [9]–[12].

In the topology proposed in [9] the VSI connected in parallel with the CSI at the motor terminal, is used for regulating the motor speed by controlling the amplitude and frequency of the VSI output and the load commutation is achieved by adjusting the firing angle of the CSI. The VSI in the topology presented in [10] is used as a current controlled active filter for compensating the reactive power as well as the harmonics currents of the CSI thereby achieving safe commutation and sinusoidal motor voltage and currents. However both the topologies presented in [9] and [10] require separate DC source for the VSI in addition to an interfacing reactor for connecting the VSI to the motor terminals making the system bulky and expensive. The topology presented in [11] is a hybrid system consisting of a CSI, a VSI and a buck converter. The VSI is used for reactive power compensation as well as harmonic filtering. The VSI in this topology also uses an interfacing inductor but does not require a separate DC source. The uncontrolled diode bridge rectifier acts as DC source for both the CSI and the VSI. However this scheme necessitates a buck converter for feeding a variable voltage to the CSI making the system more complex. In addition, since diode bridge rectifier is used for AC to DC conversion, regenerative capability of the drive system is lost. Load commutation is achieved in the scheme proposed in [12] by specially designing a motor called active-reactive induction machine with two sets of three-phase windings on the stator. One set of windings connected to CSI is made to carry active power whereas the other set of windings connected to a VSI with a LC filter is used for field excitation. This scheme however cannot be used for normal induction motors.

The concept of realization of multilevel voltage profile in an induction motor with open-end stator windings using two inverters connected at both ends of the stator windings was first introduced by Stemmler and Guggenbach in the year 1993 [13]. Since then a number of new topologies of voltage source multilevel inverters for induction motors with open-end stator windings have been proposed as reported in the literature [14]-[23]. In this paper detailed experimental results and analysis of a new scheme for realization of load commutated SCR based current source inverter fed induction motor drive with open-end stator winding is presented. This scheme can be implemented for any induction motor by accessing both ends of the stator winding which are normally available at terminal box in all medium and high power induction motors. The topology presented in this paper has a SCR based CSI connected at one end of the stator windings for feeding active power to the motor and a capacitor fed IGBT based VSI is connected at the other end of the stator windings for supplying reactive power as shown in Fig.1. Load commutation of the SCRs of the CSI is achieved by controlling the VSI in such a way that it over-compensates the reactive power required by the motor so that at the CSI terminals the current leads ahead of the voltage. This scheme does not require any interfacing inductor or separate DC source for the VSI and can be implemented for any induction motor by accessing both ends of the stator windings. This topology is also free from problems like commutation failure at low speeds normally encountered in CSI fed high power synchronous motor drives. The proposed drive system is also capable of operating in all the four quadrants with easy regeneration.

The remaining part of this paper is organized as follows. Section-II describes the power circuit diagram and operation of the proposed scheme. Control scheme of the proposed topology is given in section-III. Experimental results are given in section-IV and the conclusion in section –V.

II. POWER CIRCUIT DIAGRAM OF THE PROPOSED SCHEME

The power circuit diagram of the proposed scheme is giveninFig.1. It consists of a SCR based current source inverter at one end of the stator winding and an IGBT based capacitor fed voltage source inverter at the other end of the stator windings. The current source is realized using a SCR based controlled rectifier with an inductor at the output. A closed loop control scheme regulates the output of the current source by employing firing angle control of SCRs. The CSI is constructed using normal converter grade SCRs. The CSI switched at fundamental frequency, is operated in 120° conduction mode, resulting in a quasi-square wave current (I_{CS})as shown in Fig.2.

The SCRs of the CSI do not require any external circuit for commutation. As explained in the subsequent sections they are naturally commutated due to the leading power factor at the CSI terminals created by the operation of the VSI.

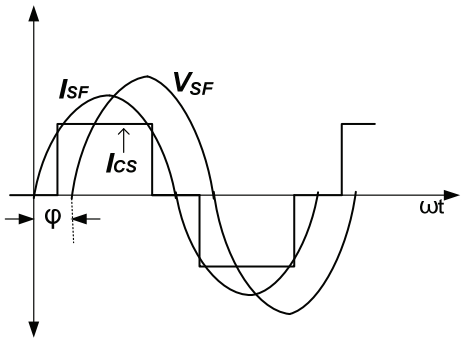

Fig.2 Current and voltage waveforms of the CSI

The voltage source inverter is constructed using fully controlled switching devices like IGBTs. The VSI is controlled in such a manner that it supplies only the reactive power required for maintaining a leading power factor at the CSI terminals. Since the VSI is not supplying any active power it does not require a DC power source. Hence a pre-charged capacitor is sufficient to feed voltage to the VSI, in ideal situation. But in a practical VSI there will be switching and conduction losses in the switching devices and dielectric loss in the capacitor. These losses cause dip in the voltage across the capacitor. Hence a small amount of active power has to be drawn from the CSI in order to compensate for these losses and to maintain the VSI capacitor voltage at the required level. A closed loop control scheme is employed for maintaining the capacitor voltage at its reference value. Since the entire reactive power is supplied by the VSI, the current source inverter feeds only the active power required by the motor. Efficiency is a major concern in high power applications. Efficiency of the load commutated SCRs based CSI drive is high due to the reduced switching and conduction losses resulting from fundamental frequency switching and the low ON state voltage drop of the SCRs (1.3V to 1.5V even for high voltage SCRs) [4]. The proposed topology is also cost effective solution to high power drive applications since converter grade SCRs are used for both rectification and inversion.

III. THE CONTROL SCHEME

The main objective of the control scheme is to make the voltage at the CSI terminals lagging behind the current so that the SCRs of the inverter are naturally commutated under all conditions of operation of the motor. The phase relationship between the fundamental components of the CSI current (I_{SF}) and the voltage (V_{SF}) to be attained for load commutation is depicted in Fig.2. The required lead angle (φ) of the current with respect to the voltage is determined based on the turn OFF time of the SCR. The VSI should be controlled in such a way that adequate reactive power is supplied to maintain this angle (φ) between the CSI terminal voltage and the current to facilitate load commutation under all conditions of operation. The CSI terminal (V_{SF}) is the vector sum of VSI voltage (V_V) the motor voltage (V_M) as given in equation (1).

$$\boldsymbol{V}_{SF} = \boldsymbol{V}_M + \boldsymbol{V}_V \qquad (1)$$

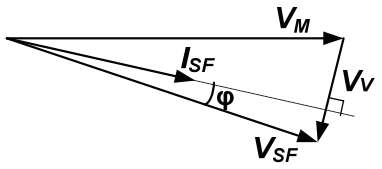

Fig.3 Phasor diagram depicting the method of achieving leading power factor at CSI terminals.

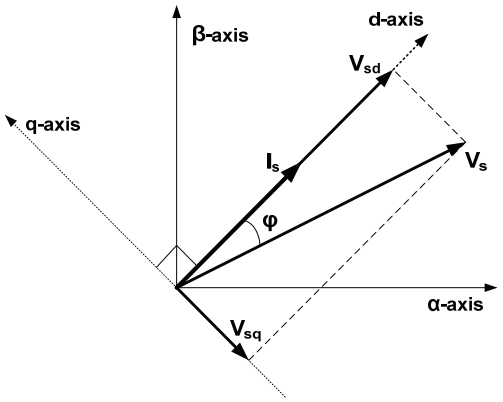

Fig.4 Generation of q-axis reference for control of the VSI

In order to attain leading power factor at the CSI terminals V_{SF} should lag behind I_{SF} as depicted in the phasor diagram given in Fig.3. Since the motor back EMF changes with speed, the VSI voltage (V_V) has to be controlled to make the CSI terminal voltage lag behind the motor current always. The control scheme for VSI is implemented on a synchronously rotating d-q reference frame with d-axis aligned with the CSI current space vector (I_S) and the q-axis perpendicular to it as shown in Fig.4. Vsd and Vsq are the components of the CSI voltage space vector (Vs) along d-axis and q-axis respectively. The block diagram of the VSI control scheme is shown in Fig.5.The CSI terminal voltages are sensed and transformed into stationary (α – β) reference frame using Clark's transformations to obtain voltages along the two orthogonal

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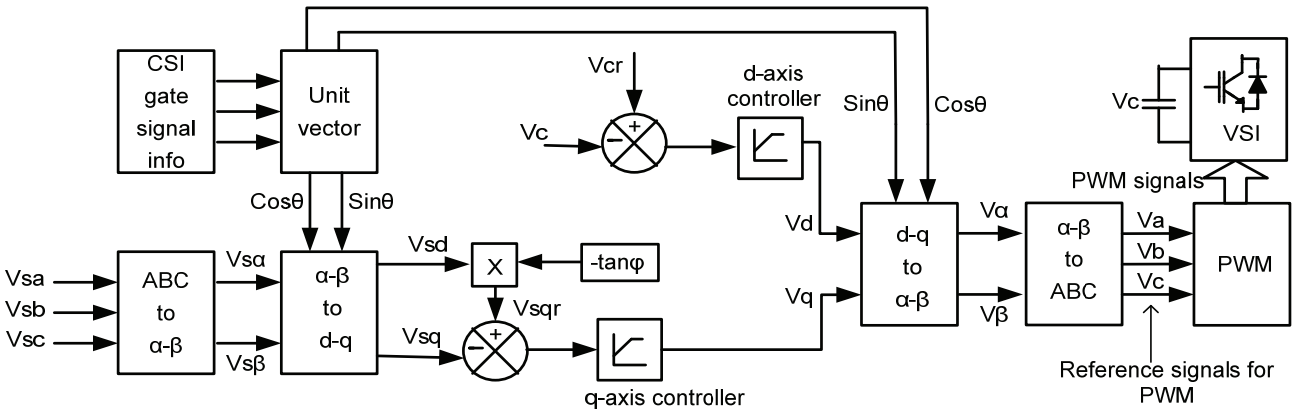

Fig.5 Control Scheme of the Voltage Source Inverter

axes (Vsα and Vsβ). The voltages Vsα and Vsβ are then transformed to synchronously rotating reference frame orientated with CSI current space vector using Park's transformations to obtain the voltages Vsd and Vsq along d-axis and q-axis respectively. The unit vectors required for these transformations are generated using the information of the gating signals of the CSI. Two controllers, one on q-axis and the other on d-axis are implemented for the closed loop control of the VSI as described in the subsequent sections.

q-axis controller:

The q-axis controller compares the q-component of the inverter voltage (Vsq) vector with the q-axis reference voltage (Vsqr) and the error is processed through a proportional plus integral (PI) controller to generate the q-axis reference voltage for VSI operation (Vq). Fig.4 shows the magnitude and direction of Vsq for leading power factor operation of the CSI. From this figure the q-axis reference voltage (Vsqr) can be obtained as given in the equation (2).

$$Vsqr = -Vsd \times \tan(\varphi) \quad (2)$$

d-axis controller:

As stated in section II, the VSI is not used for supplying active power to the motor. Its role is only to provide adequate reactive power to maintain a leading power factor at CSI terminal. Hence a pre-charged capacitor is sufficient to provide the required voltage for the VSI. A closed loop control scheme with a PI controller is employed for the control of capacitor voltage as depicted in Fig.5. The voltage across the capacitor (Vc) is sensed and compared with its reference value (Vcr) and a PI controller is used to make this error zero. The output of the PI controller gives the required d-axis reference voltage (Vd) for the operation of the VSI.

The reference voltages in d-q frame (Vd and Vq) are then transformed back to (α – β) reference frame using inverse Park transformation and then to three phase reference voltages using inverse Clark's transformation. These three-phase reference voltage waveforms are used for the pulse width modulation of the VSI to generate the required voltage for making the CSI terminal voltage lagging behind the current. Since the unit vectors for these transformations are derived from the gating signals of the CSI both the VSI and the CSI operate at the same fundamental frequency. The complete control scheme of the VSI is depicted in Fig.5.

Pre-charging of the capacitor:

The proposed scheme does not require a separate circuit for pre-charging of the VSI capacitor. The capacitor can be pre-charged by simply turning ON the upper SCR in any one leg and the lower SCR in another leg of the CSI. The capacitor will be charged by the DC link current through the turned ON SCRs and the reverse diodes in the IGBTs of the corresponding legs of the VSI as shown in Fig. 6. The capacitance value (C) can be decided based on the formula given below.

$$C = Id(rated)/(Fs*\Delta V) \quad (3)$$

where Id(rated) is the rated dc link current, Fs is the switching frequency of the VSI and the ΔV is the allowable ripple voltage.

Control of DC link current and switching frequency of CSI :

The required DC link current reference and the switching frequency of the current source inverter are decided by a closed loop control scheme as shown in Fig.7. The outer speed loop decides the reference value for DC link current.

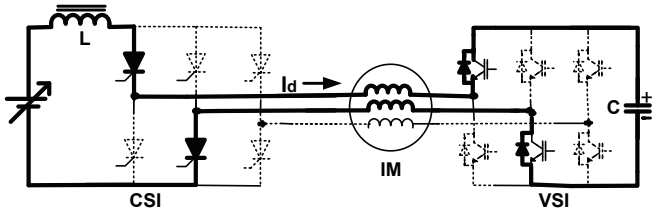

Fig.6 Pre-charging of the VSI capacitor.

The inner current control loop compares the actual DC link current with the reference current and the firing angle of the rectifier is controlled to maintain the DC link current at the desired value. The speed control loop with a slip limiter decides the switching frequency of the current source inverter.

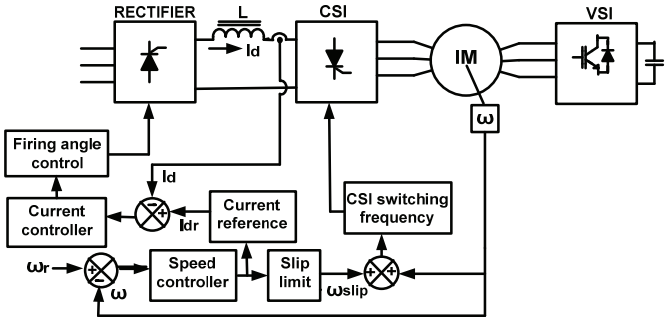

Fig.7 Control scheme for the CSI

IV. EXPERIMENTAL VERIFICATION

The experimental verification of the proposed scheme was carried out on a laboratory prototype consisting of a SCR based fully controlled rectifier, DC link reactor, SCR based CSI, induction motor with open-end stator winding (1.5HP, 400V, 50Hz) and an IGBT based VSI. The motor parameters are given below.

Rated power = 1.5hp, No of poles P=4
Inertia (J) =0.01 Kg.m^2,Stator Resistance (Rs) =8.89 Ω
Rotor Resistance (Rr) = 5.51 Ω,
Stator inductance (L_s) =24.36 mH
Rotor inductance (L_r) =24.36 mH
Magnetising inductance (L_m) = 450.46 mH.

The inductance of DC link reactor was 200 mH. In the experimental set up a DC capacitor of value 2200μF was used for the VSI. The reference value of the voltage across the VSI capacitor was 75V. The VSI was switched at 2000Hz. The entire control scheme was implemented on a digital signal controller (TMS320F28335). The DC link current, DC capacitor voltage and the motor voltages were sensed using Hall effect sensors. A block diagram of the implementation scheme is given in Fig.8.

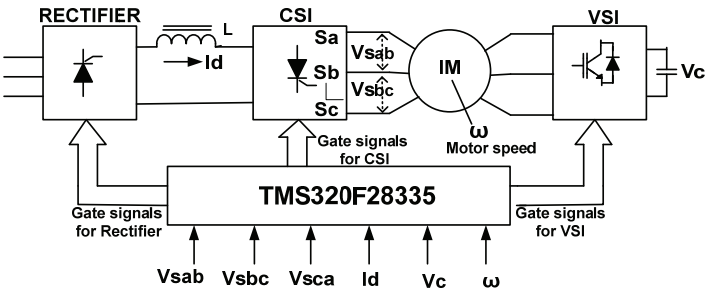

Fig.8 Implementation of the control scheme.

The experimental results showing the motor current, motor voltage, DC link current and VSI capacitor voltage for different conditions of operation of the motor for phase-A are given in figures 9 to 16. Fig.9 shows the waveforms when the CSI is operating at 40Hz at no-load. It is evident from the waveform of the motor current that the SCRs of the CSI are commutated properly. It can also be seen that the voltage across the VSI capacitor is well-balanced, proving the effectiveness of the capacitor voltage control algorithm. Similar experimental results when the motor is operating at 30Hz, 20Hz and 10Hzare given in Fig.10, Fig.11 and Fig.12 respectively.

A major problem encountered by load commutated CSI fed synchronous motor drives used in high power applications is the commutation failure at low speeds since the back EMF generated is not sufficient to turn OFF the SCRs. The proposed topology is free from such issues and can operate at very low speeds without help of any external commutation circuit. This feature of the proposed scheme is experimentally verified by operating the drive at 6Hz and 3Hz and the results are given in Fig.13and Fig.14 respectively.

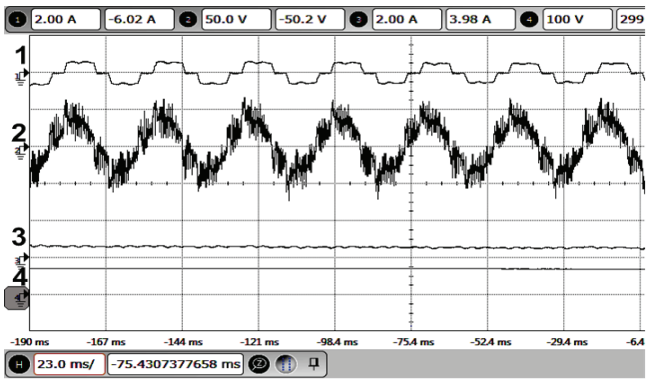

Fig.9 Voltage and current waveforms at 40 Hz operation. X-axis: 23ms/div.1. Motor current (Y- axis : 2A/div.). 2. Motor voltage (Y-axis:50V/div.). 3. DC link current (Y-axis: 2A/div). 4. VSI capacitor voltage(Y-axis: 100V/div).

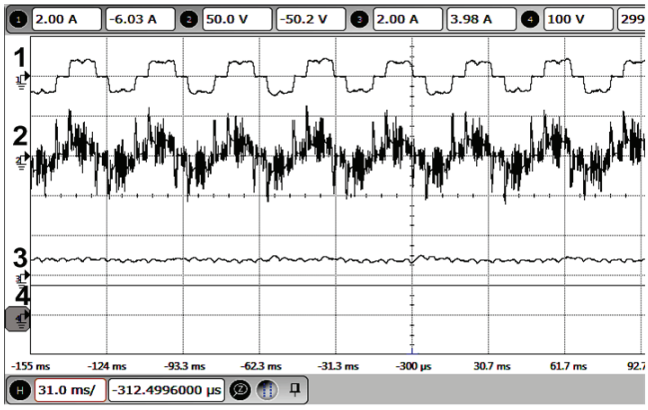

Fig.10 Voltage and current waveforms at 30 Hz operation: X-axis: 31ms/div.1. Motor current(Y axis : 2 A/div.). 2.Motor voltage (Y-axis:50V/div.). 3. DC link current (Y-axis: 2 A/div.). 4. VSI capacitor voltage (Y-axis: 100V/div.).

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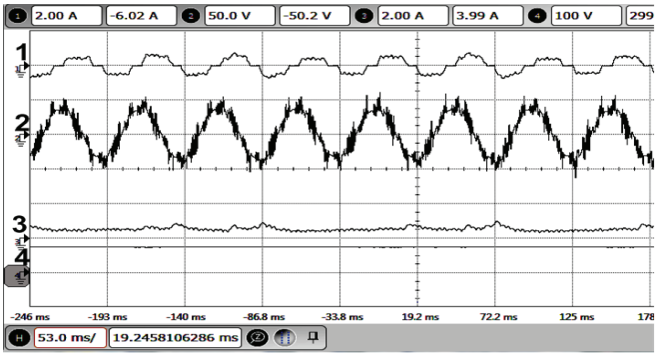

Fig.11 Voltage and current waveforms at 20 Hz operation: X-axis: 53ms/div.1. Motor current(Y- axis : 2A/div.). 2.Motor voltage(Y-axis:50V/div.) 3. DC link current: (Y-axis:2A/div.). 4. VSI capacitor voltage(Y-axis: 100V/div.).

It can be seen from all these waveforms that SCRs of the CSI are commutated properly and the VSI capacitor voltage remains balanced.

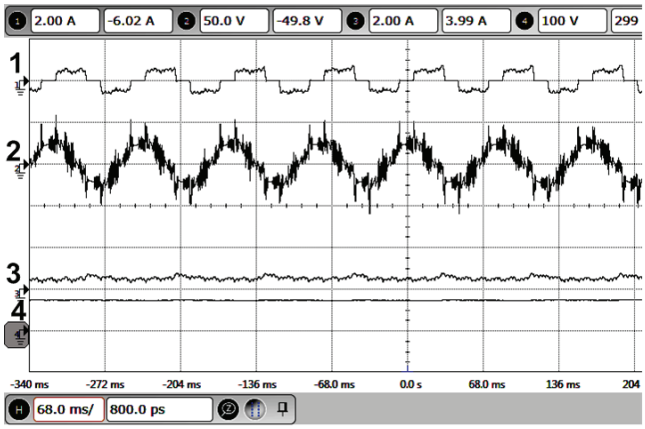

Fig.12 Voltage and current waveforms at 10 Hz operation: X-axis: 68ms/div. 1. Motor current (Y axis : 2A/div.). 2.Motor voltage (Y-axis:50V/div.). 3. DC link current (Y-axis: 2A/div.). 4. VSI capacitor voltage (Y-axis: 100V/div.).

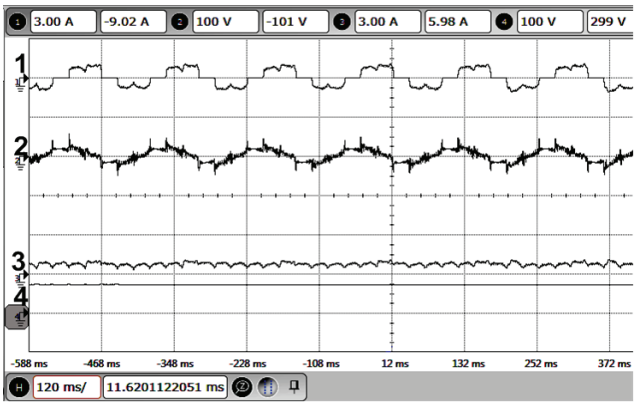

Fig.13 Voltage and current waveforms at 6 Hz operation: X-axis: 120ms/div. 1. Motor current (Y- axis : 3A/div.). 2.Motor voltage (Y-axis:100V/div.). 3. DC link current (Y-axis: 3A/div.). 4. VSI capacitor voltage (Y-axis: 100V/div.).

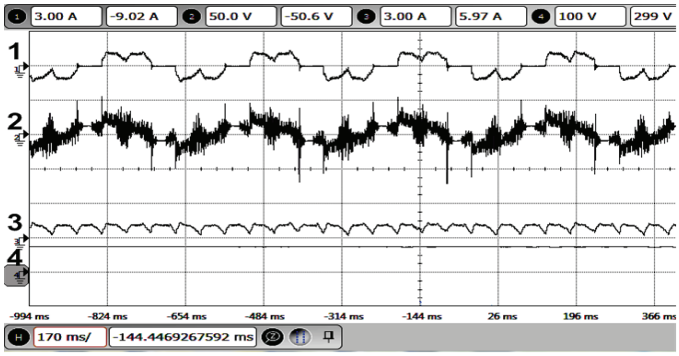

Fig.14 Voltage and current waveforms at 3 Hz operation: X-axis: 170ms/div. 1. Motor current (Y- axis : 3A/div.). 2.Motor voltage (Y-axis: 50V/div.). 3. DC link current (Y-axis: 3A/div.). 4. VSI capacitor voltage (Y-axis: 100V/div.).

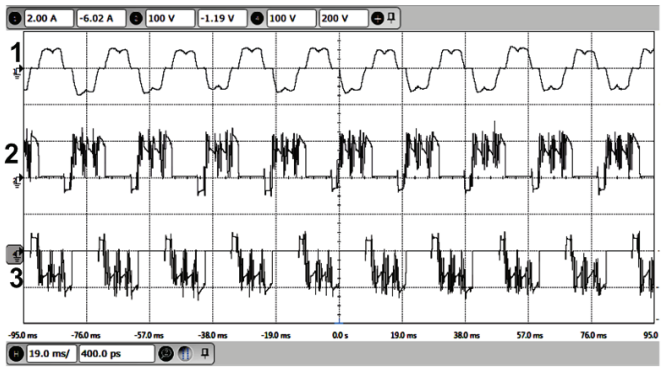

Fig.15. CSI current and SCR voltage waveforms at 50 Hz operation (phase-A): X-axis: 19ms/div. 1. CSI current (Y- axis : 2A/div.). 2.Voltage across top SCR (Y-axis: 100V/div.). 3. Voltage across bottom SCR (Y-axis: 100V/div.)

The experimental results showing the CSI current, voltage across top and bottom SCRs of phase-A during 50 Hz operation are given in Fig.15. This result demonstrates the commutation of the top and bottom SCRs of a leg of the CSI. The reverse voltage appearing across the SCRs at the time of commutation is clearly visible in this figure. Performance of the scheme during transient condition was verified by accelerating the drive from 20Hz to 50 Hz and the results are given in Fig.16. It is evident that the capacitor voltage remains balanced even during transient conditions. As explained in the previous section the VSI capacitor can be pre-charged by simply turning ON one upper SCR and one lower SCR in any two legs of the CSI. Normal operation of the control scheme starts when the voltage across the capacitor is reaches its reference value. Pre-charging of the VSI capacitor is demonstrated in the experimental result given in Fig.17.Waveforms depicting the performance of the drive during sudden change in the load are given in Fig.18. Fig.19 shows response of the drive to a step change in speed reference. Steady state waveforms of V_{sd},V_{sq}, V_d and V_q are given in Fig.20.A photograph of the experimental set-up is shown in Fig.21.

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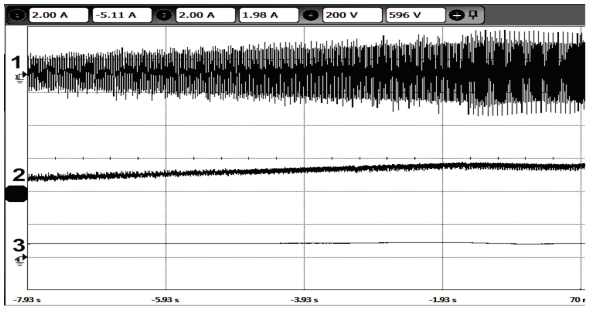

Fig.16 Voltage and current waveforms during acceleration of the motor from 20Hz to 50Hz: X-axis: 2s/div. 1. Motor current (Y- axis : 2A/div.). 2. DC link current (Y-axis: 2A/div.).3. VSI capacitor voltage (Y-axis: 200V/div.).

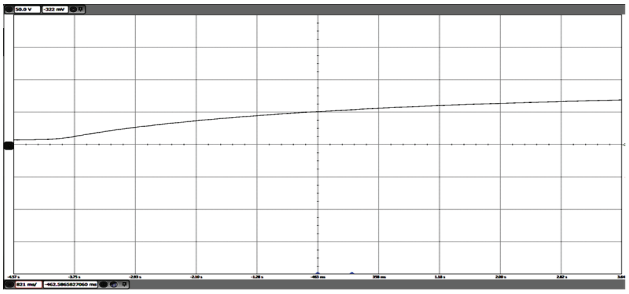

Fig.17 Pre-charging of capacitor. X-axis: 821 ms/div., Y-axis :50V/div.

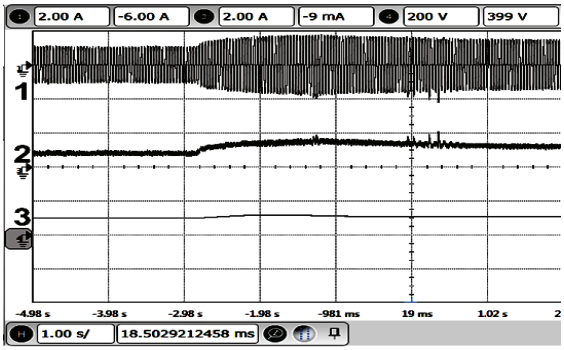

Fig.18 Waveforms during sudden change in the load: X-axis: 1s/div. 1. Motor current (Y- axis : 2A/div.). 2. DC link current (Y-axis: 2A/div.). 3. VSI capacitor voltage (Y-axis: 200V/div.).

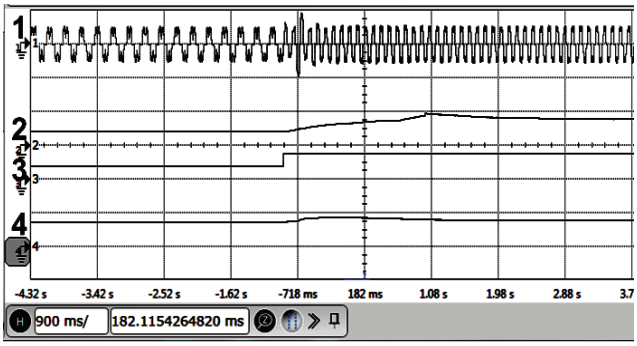

Fig.19 Waveforms during step change in speed reference from 300 RPM to 600 RPM: X-axis: 900ms/div. 1. Motor current (Y- axis : 2A/div.). 2. Actual speed of the motor (Y-axis: 200 rpm/div.). 3. Reference speed (Y-axis: 200 rpm/div.). 4. VSI capacitor voltage (Y-axis: 100V/div.).

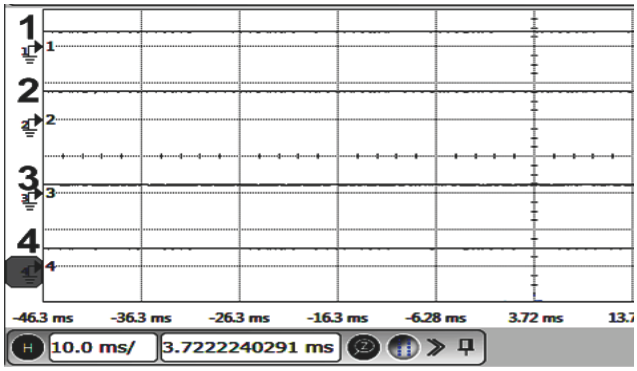

Fig.20 Steady state waveforms of V_{sd}, V_{sq}, $V_d$and V_q. X-axis: 10ms/div. 1. V_{sd} (Y- axis:60V/div.). 2. V_{sq} (Y- axis : -60V/div.). 3. V_d (Y- axis: 10V/div.). 4. V_q (Y- axis : -100V/div.).

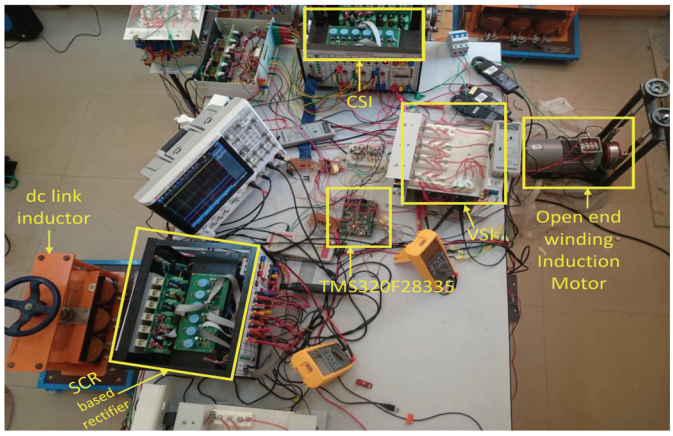

Fig.21 Photograph of the experimental setup

V. Conclusion

A new topology for SCR based load commutated CSI fed induction motor drive with open-end stator winding is presented in this paper. The proposed scheme uses a capacitor-fed voltage source inverter connected at one end of the stator winding to make the power factor leading at the terminals of the CSI connected at the other end of the stator windings. Since the CSI current leads ahead of the CSI terminal voltage under all conditions of operation of the motor the SCRs of the CSI are naturally commutated. The CSI supplies the entire active power required by the motor. The VSI in this scheme supplies only the reactive power required to maintain slightly leading power factor at the CSI terminals and hence the power handled by the VSI is only 20 to 25% of that of the CSI, for high power motors. The CSI is switched at fundamental frequency and hence the switching losses are considerably reduced compared to that of pulse width modulated inverters. This reduction in switching loss is significant in high power applications. The experimental results demonstrate the ability of the proposed drive scheme to operate at very low speed without any external commutation circuit. This is a significant advantage compared to the CSI fed synchronous motor drives which experience commutation failure at low speed due to insufficient back EMF. Since induction motors are more rugged, reliable, efficient and cheaper than synchronous motors the proposed scheme has the potential to be considered for very high power applications where load commutated CSI

fed synchronous motor drives are in use at present. The experimental results given in the paper validate the proposed topology and control scheme under transient as well as steady state operating conditions.

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