Extendable Non-isolated High Gain DC-DC Converter Based on Active-Passive Inductor Cells

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***Abstract*— In this paper, a new non-isolated high step-up dc-dc converter is proposed. Active-passive inductor cells (APICs) is used to extend the topology. The ability to achieve high gains is the main merit of the proposed topology. The proposed converter operates based on parallel charging and series discharging of the inductors. The converter also achieves high step-up voltage gain with appropriate duty cycle and low voltage and current stress on the power switches and diodes. The proposed converter is analyzed in operation modes. The main parameters of the converter such as voltage gain, voltage stress of semiconductor devices are calculated to compare with other structures in literature. Considering the output voltage ripple and filter size, the proposed converter is designed. Moreover, the losses and efficiency of the converter are calculated. The performance of the proposed converter is validated by experimental results.**

***Index Terms*— High gain dc-dc converter, Active-passive inductor cell, High voltage gain, Output voltage ripple (OVR)**

I. Introduction

In spite of effective environmental and economic aspects of renewable energy sources (e.g. photovoltaic (PV) and wind generation), there are some limitations about utilization of these sources. Low output voltage is one of them. In order to eliminate the limitations, high step-up dc-dc converters have been used [1-4]. However, the quality of the input current waveform and lower costs of design and operation are the main issues related to high gain dc-dc converters [5-7]. Considering these issues, and voltage stresses of the semiconductor devices, conduction losses, and the number of components are being investigated. In addition to these parameters, the size of the passive elements and their effect on quality of the output voltage is analyzed. Some topologies have been proposed for high step-up dc-dc converters in the literature [8-11]. The articles which follow two main objectives: First, high voltage gain for a logical value of duty cycle and second, a converter with high efficiency and low voltage stress of devices. Isolated dc-dc converters were the primary solution for these objectives. In these converters, conduction losses and voltage stresses of the switches are increased due to leakage inductance. Using complicated zero voltage switching (ZVS) and zero current switching (ZCS) methods and coupled inductors can improve the negative effect of the leakage inductance [12-15]. In coupled inductor converters, the transforming feature of the mutual inductors is similar to the isolated dc-dc converters. The secondary winding of the mutual inductors is like a voltage source and leads to the increase in the voltage gain of the converter. The voltage gain of the converter is a function of the turns of the mutual inductors. In topologies based on coupled inductors, because of the higher inductance of the converter, transient response time is increased in high voltage gains [14]. The structures based on switched capacitor (SC) are the non-isolated structures that have been presented [15] and [16]. In these structures, due to the deficiency of electromagnetic elements, corresponding problems are accordingly eliminated. The problem related to the extreme instantaneous currents of the capacitors is the main disadvantage of the switched-capacitor structures. Moreover, the output voltage regulation capability is poor in a wide load variation because the output voltage must be a fraction or a multiplier of the input voltage. Either of the switched-capacitor (SC) or switched-inductor and boost converters can be integrated together to obtain a step-less voltage gain. A family of single-switch dc-dc converters with high voltage gain is presented in [17-20]. In these structures, simple switching dual structures, formed by either two capacitors and 2–3 diodes, or two inductors and 2–3 diodes are defined. These circuit blocks can provide either a step-down of the input voltage or a step-up of it. They are inserted in classical buck, boost, buck-boost, Cuk, Sepic, Zeta converters to provide new power supplies with a steep voltage conversion ratio. In step-up structures, the capacitors are charged in parallel when the switch is turned off and discharged in series when the switch is turned on. The inductors are charged in parallel when the switch is turned on and discharged in series when the switch is turned off. Despite the simple structure, the voltage gain is limited and the input current is discontinuous. Besides the advantages of the conventional interleaved, reduction of the input current ripple

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is the other merit of these structures. The interleaved structure can be employed to increase the power level.

In this paper, a new high gain dc-dc structure is proposed. The proposed converter is designed by combining the presented topology in [21] with APICs. It also can be extended by adding APICs to achieve high gains. The maximum accessible value of voltage gain in [21] is 10. The main merits of the proposed converter are low voltage stress of the switches, the least maximum current through the switches that result in low conduction losses.

In this paper, first, the operation modes of the proposed converter are classified by comparing the inductor current with load current. Then, the main parameters of the converter such as voltage gain, voltage and current stress of the switches and diodes are obtained. The elements of the proposed converter will be designed. The performance of the proposed converter will be analyzed under real conditions. Finally, the experimental results will be used in order to revalidate the theoretical analysis.

II. Proposed Converter

The power circuit of the proposed converter is shown in Fig. 1. The operation of this converter in continuous conduction mode (CCM) is classified into complete inductor supply mode (CISM) and incomplete inductor supply mode (IISM). Discontinuous conduction mode (DCM) just includes IISM. To simplify the analysis, all elements are assumed ideal and the capacitance of the capacitor is considered to be high and all of the inductors have the same inductance. It should be mentioned that if the inductors do not have the same inductance, the analysis of the proposed converter will be different. But the final results for main parameters will be the same as in the case that the inductances are similar. In the proposed converter, by comparing minimum current of the inductors with load current, CISM and IISM operations are determined. In CISM, the minimum current of inductors is more than the load current, while in IISM, the minimum current of inductors is less than the load current. The equivalent Circuit of the proposed converter in on and off states and the waveforms of the voltage and current of the elements are shown in Figs. 2 and 3, respectively.

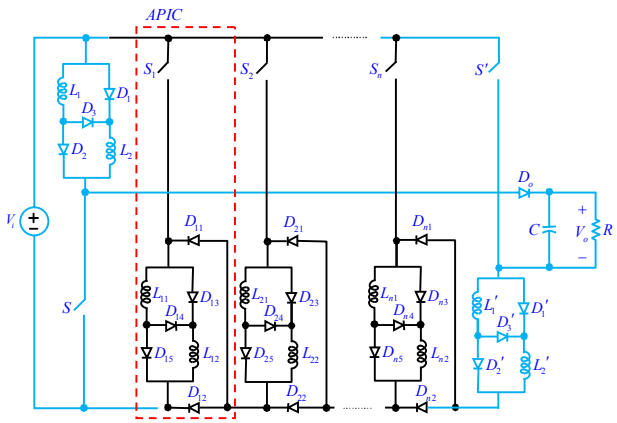

Fig 1. Proposed converter

III. Analysis the Proposed Converter

A. Analysis of the proposed converter in CCM

Time interval of T_{on}: States of the switches and diodes are given in Table I. The equievalant circuit of the proposed converter in T_{on} is shown in Fig. 2(a). In this time interval is same for CISM-CCM and IISM-CCM. The voltage across the inductors is given by:

$$v_L = V_i \tag{1}$$

Current through the inductors is as follows:

$$i_L = \frac{V_i}{L}t + I_{LV} \tag{2}$$

By considering (2), during this time interval, the inductors are charged and the current through them is increased so that in $t = DT$, the current of the inductors will be at its maximum value. By Applying $t = DT$ in (2), the maximum current of the inductors is obtained as follows:

$$I_{LP} = \frac{V_i DT}{L} + I_{LV} \tag{3}$$

During this time interval, the capacitor provides load current and the capacitor current equals to $(-I_o)$ (Fig. 2(a)). At the end of this time interval, the energy stored in the capacitor is discharged, so it causes the capacitor voltage to decrease to the value of V_{CV}.

Time interval of T_{off}: States of the switches and diodes are given in Table I. The equivalent circuit of the proposed converter in this time interval is shown in Figs. 2(b) and 2(c).The voltage across the inductors is as follows:

$$v_L = \frac{V_i - V_o}{2n+4} \tag{4}$$

where n is the number of APICs.

During the interval of T_{off}, assuming $t_1 = 0$ as the new time reference, the current of the inductors is given by:

$$i_L = \frac{V_i - V_o}{(2n+4)L}t + I_{LP} \tag{5}$$

When the inductors are discharged, the current through them is decreased, so that at the end of this interval, it will be equal to I_{LV}.

By applying $t = (1-D)T$ in (5), the minimum current through the inductors is as follows:

$$I_{LV} = \frac{(V_i - V_o)(1-D)T}{(2n+4)L} + I_{LP} \tag{6}$$

The capacitor current is obtained as follows:

$$i_C = \frac{V_i - V_o}{(2n+4)L}t + I_{LP} - I_o \tag{7}$$

Considering (7), currents of the capacitor and inductors decrease at this time interval (Fig 3(a)). The inductors provide load current along with charging the capacitor. During T_{off}, the capacitor is charged and its voltage increases from V_{CV} to V_{CP}. The time interval T_{off} in IISM-CCM is divided into time intervals of (t_1, t_2) and (t_2, t_3) as follows:

Time interval of (t_1,t_2) : From (6), as i_L decreases i_C will decrease and reach zero at the moment of t_2 .considering (7) t_2 is as follows:

$$t_2 = \frac{(I_{LP} - I_o)(2n+4)L}{(V_o - V_i)} \tag{8}$$

The equivalent circuit of the proposed converter in this time interval is shown in Fig. 2(b)

Time interval of (t_2,t_3) : By considering Fig. 4(b) and (7), i_C also decreases same as i_L . The capacitor current decreases to $I_{LV} - I_o$ at t_3 .The inductor and capacitor provide the load current together at this time interval (Fig. 2c)

Voltage gain Calculation

By applying the volt-second balance law, and considering (1) and (4), the voltage gain is obtained as follows:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{1+(2n+3)D}{1-D} \tag{9}$$

Fig. 4 shows the variation of voltage gain versus duty cycle and n , in CCM. It is obvious that for certain values of the duty cycle, as the value of n decreases, the voltage gain will increase.

TABLE I
STATES OF SWITCHES AND DIODES

Device	T_{on}	T_{off}
$S, S', S_1, S_2, \ldots, S_n$	on	off
D_o	off	on
D_1 , D_2 , D_1' , and D_2'	on	off
$D_{11}, D_{21}, \ldots, D_{n1}$	off	on
$D_{12}, D_{22}, \ldots, D_{n2}$	on	off
$D_{13}, D_{23}, \ldots, D_{n3}$	on	off
$D_{15}, D_{25}, \ldots, D_{n5}$	on	off
D_3 , and D_3'	off	on
$D_{14}, D_{24}, \ldots, D_{n4}$	off	on

Voltage stress of the diodes and switches

The normalized voltage stress of the diodes and switches versus output voltage are given in Table II.

B. Analysis of the proposed converter in DCM

This mode is divided into four time intervals.

Time interval of T_{on}: Analysis of proposed converter at this time interval is same as CCM which was mentioned earlier. By applying $I_{LV} = 0$ and $t = DT$ in (3), the maximum current through the inductors is obtained as follows:

$$I_{LP} = \frac{V_i DT}{L} \tag{10}$$

Time interval T_{off}: This time interval is divided into three time intervals; (t_1,t_2) , (t_2,t_{2a}) , and (t_{2a},t_3) . The energy transmission process during these time intervals is as follows:

Time interval of (t_1,t_2) **:** At this period of time, currents of the inductors and capacitor can be obtained from (5) and (7). The energy transmission process is the same as CCM during the time interval (t_1,t_2) (Fig. 2b). In this time interval, t_2 is same as (8)

Time interval of (t_2,t_{2a}) **:** The energy transmission process is the same as the CCM during the time interval (t_1,t_2) with a difference, that the inductors' current is zero at $t = t_{2a}$. During this time, capacitor's current equals the load current. According to Fig. 2(c), the capacitor voltage decreases as the capacitor energy is discharged (Fig. 4(c)). Considering Fig. 4(c) and (8), t_{2a} is as follows:

$$t_{2a} = \frac{I_{LP}(2n+4)L}{(V_o - V_i)} \tag{11}$$

By assuming $t_1 = 0$ as the new time reference, maximum current through the inductors is as follows:

$$I_{LP} = \frac{(V_o - V_i)D'T}{(2n+4)L} \tag{12}$$

By applying (9) in (10), D' is given by:

$$D' = \frac{(2n+4)V_i D}{(V_o - V_i)} \tag{13}$$

Time interval of (t_{2a},t_3) **:** At this time interval, the capacitor current equals $(-I_o)$. The capacitor alone provides the load current. The capacitor's voltage decreases as the capacitor's energy is discharged (Fig. 4(c)).

Voltage gain calculation

By using the current-second balance law for the capacitor, voltage gain in DCM is obtained as follows:

$$\frac{V_o}{V_i} = \frac{1}{2} + \sqrt{\frac{(n+2)RD^2}{2Lf} + \frac{1}{4}} \tag{14}$$

TABLE II
THE VOLTAGE STRESS OF DIODES AND SWITCHES

S	$\frac{n+1+M_{CCM}}{(n+2)M_{CCM}}$
S'	$\frac{1+(n+1)M_{CCM}}{(n+2)M_{CCM}}$
Switch of j th cell	$\frac{(n-j+2)+jM_{CCM}}{(n+2)M_{CCM}}$
D_o	$\frac{1+M_{CCM}}{M_{CCM}}$
Diodes D_1 and D_4 of j th cell and D_3 , and D_3'	$\frac{1}{M_{CCM}}$
Diode D_2 of j th cell	$\frac{M_{CCM}-1}{(n+2)M_{CCM}}$
Diodes D_3 and D_5 of j th cell and D_1 , D_2 , D_1' , and D_2'	$\frac{M_{CCM}-1}{(2n+4)M_{CCM}}$

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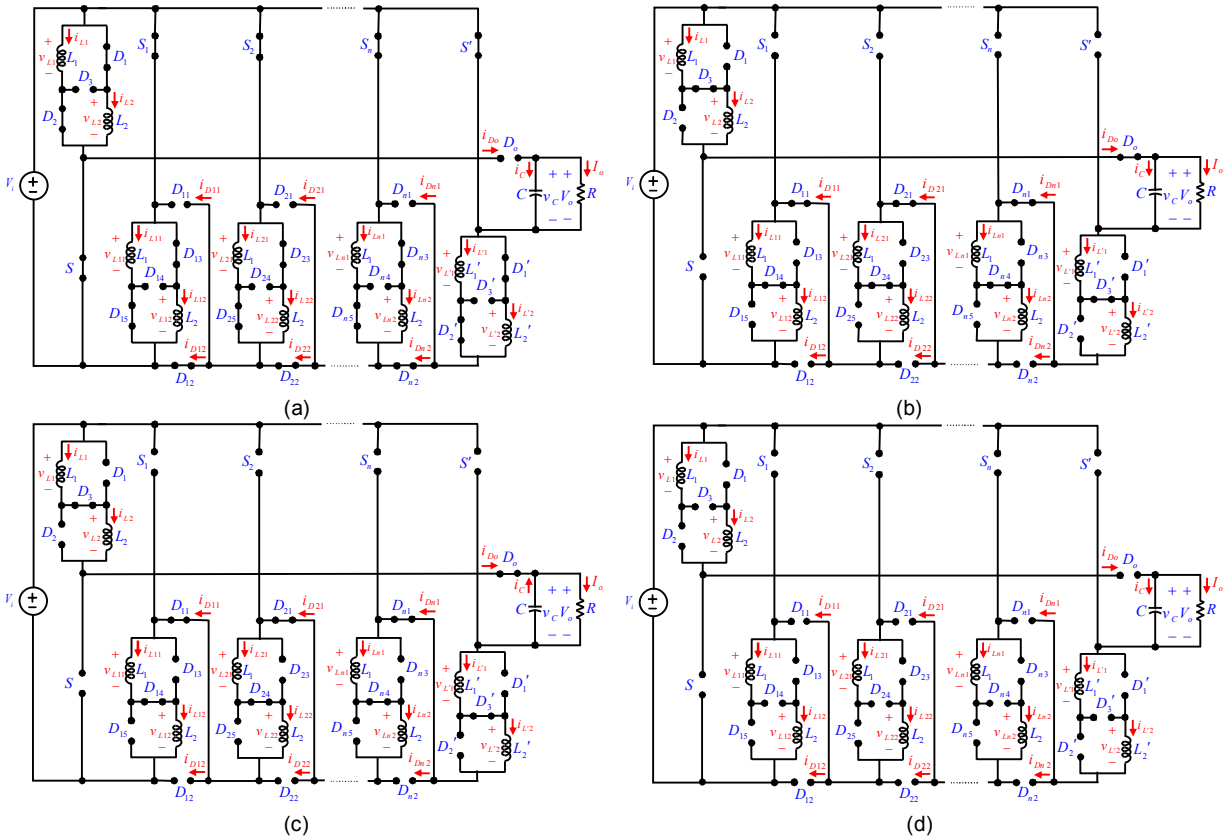


Fig 2. Operational modes of the proposed converter. (a) T_{on}. (b) T_{off} $(I_{LV} > I_o)$. (c) T_{off} $(I_{LV} < I_o)$. (d) T_{off} $(i_L = 0)$

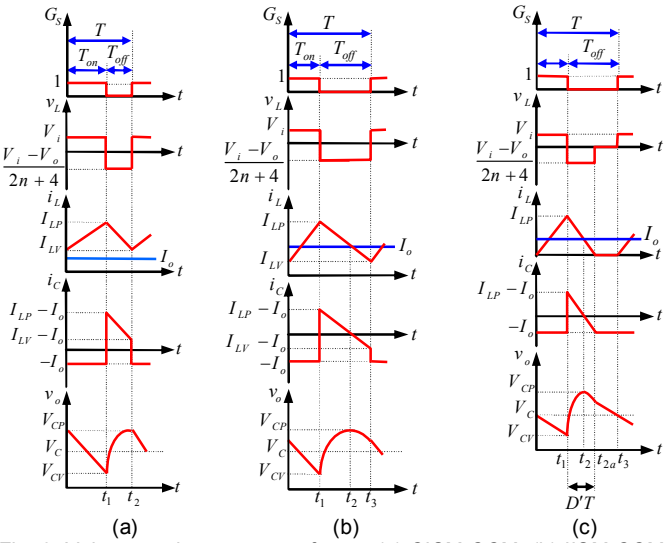


Fig. 3. Voltage and current waveforms. (a) CISM-CCM. (b) IISM-CCM. (c) IISM-DCM

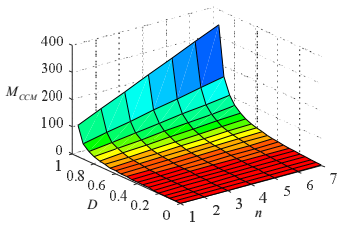


Fig. 4. Variation of voltage gain versus duty cycle and n

IV. Critical Conduction Mode

The minimum current through the inductors is as follows:

$$I_{LV} = I_o\left[\frac{1}{1-D} - \frac{RD}{2Lf}\frac{(1-D)}{[1+(2n+3)D]}\right] \tag{15}$$

By applying $I_{LV} = 0$ and $I_{LV} = I_o$ in (13), the critical inductance between (CCM and DCM) and (CISM and IISM) are obtained as follows, respectively:

$$L_C = \frac{(n+2)(V_o - V_i)V_i^2 R}{fV_o[(2n+3)V_i + V_o]^2} \tag{16}$$

$$L_K = \frac{(n+2)RV_i^2}{fV_o[(2n+3)V_i + V_o]} \tag{17}$$

V. OVR and Maximum Current of Switches

The output voltage ripple and maximum current of the switches are two parameters that have the main role in the operation of a dc-dc converter as well as the voltage stress of the switches. These parameters are calculated as follows.

A. Output Voltage Ripple

The output voltage ripple in CISM can be determined by integrating the capacitor current over the time interval T_{on} and also it can be determined in IISM-CCM and IISM-DCM, by integrating the capacitors current over (t_1, t_2).

The OVR in the operational modes of the converter is obtained as Table III. The output voltage ripple is independent of inductance values in CISM-CCM and is reversely related to

V_i and R . The ratio of the output voltage ripple variations is reversely related to inductance, V_i and R values in IISM-CCM and IISM-DCM.

TABLE III
OUTPUT VOLTAGE RIPPLE IN THE OPERATIONAL MODES

CISM-CCM	$V_{PP}^{CISM-CCM} = \frac{V_o(V_o - V_i)}{fRC[V_o + (2n+3)V_i]}$
IISM-CCM	$V_{PP}^{IISM-CCM} = \frac{(n+2)(V_o - V_i)L}{C}\left[\frac{V_o}{(2n+4)V_iR} + \frac{V_i}{2Lf[(2n+3)V_i + V_o]}\right]^2$
IISM-DCM	$V_{PP}^{IISM-DCM} = \frac{(n+2)L}{C(V_o - V_i)}\left[\frac{V_o}{R} - \sqrt{\frac{V_o(V_o - V_i)}{(n+2)LfR}}\right]^2$

B. Maximum Current of the Switches and diodes

Maximum value of the current of switches equals twice the maximum current of inductors. The maximum current of switches and diodes in CCM and DCM is given in Table IV. The maximum value of i_S in CCM and the minimum value in DCM are obtained for $L = L_C$. Considering (16) in Table IV, it results that:

$$I_{SP,\min}^{DCM} = I_{SP,\max}^{CCM} = \frac{2V_o[(2n+3)V_i + V_o]}{(n+2)RV_i} \tag{18}$$

Table. IV
THE MAXIMUM CURRENT OF THE SWITCHES AND DIODES

CCM	Switches	$\frac{V_o[V_o + (2n+3)V_i]}{(n+2)RV_i} + \frac{(V_o - V_i)V_i}{Lf[V_o + (2n+3)V_i]}$
	All diodes	$\frac{V_o[V_o + (2n+3)V_i]}{(2n+4)RV_i} + \frac{(V_o - V_i)V_i}{2Lf[V_o + (2n+3)V_i]}$
	Diode D_2 of j th cell	$\frac{(n-j+1)V_o[V_o + (2n+3)V_i]}{(n+2)RV_i} + \frac{(n-j+1)(V_o - V_i)V_i}{Lf[V_o + (2n+3)V_i]}$
DCM	Switches	$I_{SP}^{DCM} = \sqrt{\frac{4V_o(V_o - V_i)}{(n+2)RfL}}$
	All diodes	$\sqrt{\frac{V_o(V_o - V_i)}{(n+2)RfL}}$
	Diode D_2 of j th cell	$(n-j+1)\left[\sqrt{\frac{4V_o(V_o - V_i)}{(n+2)RfL}}\right]$

VI. Voltage Gain and Efficiency in Real Condition

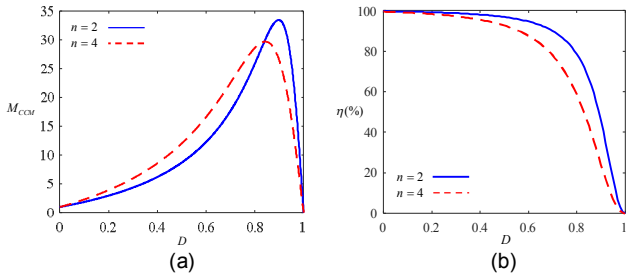
In real condition analysis, it is assumed that the current of the inductors equals its average value. The efficiency of the proposed converter can be obtained as in the following relation, by obtaining the average and RMS values of the currents through the elements and calculation of power losses:

$$\eta = \frac{1}{\left\{\frac{(n+2)(4r_sD + 2r_L)}{R(1-D)^2} + \frac{r_{Do} + Dr_C + nr_{D1} + (n+2)r_{D4}}{(1-D)R} + \frac{(2n+4)Dr_{Dj5}}{(1-D)^2R} + \sum_{j=1}^{n}\left(\frac{4D(n-j+1)^2 r_{D2j}}{(1-D)^2R}\right)\right\}} \tag{19}$$

The voltage gain is also achieved in real condition as follows:

$$\frac{V_o}{V_i} = \frac{M_{CCM}}{1 + \left\{\frac{(n+2)(4r_sD + 2r_L)}{R(1-D)^2} + \frac{Dr_C + (2n+3)r_{Do}}{(1-D)R} + \frac{(2n+4)Dr_{Dj5}}{(1-D)^2R} + \sum_{j=1}^{n}\frac{4D(n-j+1)^2 r_{Dj2}}{(1-D)^2R}\right\}} \tag{20}$$

The variation of the voltage gain and efficiency of the proposed converter versus duty cycle is shown in Fig. 5. According to Fig. 5, in real conditions and for high values of the duty cycle, by increasing duty cycle, the voltage gain will decrease.



(a) (b)

Fig. 5. Variation of (a) Voltage gain and (b) Efficiency versus duty cycle

VII. Comparison

The features and the voltage gain of the proposed converter and the presented structure in the literature are listed in Table V. Variation of the voltage gain versus duty cycle is shown in Fig. 6(a). As can be seen, the voltage gain of suggested converter for $n = 2$ and $n = 4$ is higher than the others with the same duty cycle. It is obvious that for lower duty cycles, the presented converter in [11] has the highest voltage gain. But in this condition, the converter isn't applicable in high gain applications. Variation of the normalized voltage stress of the switches versus voltage gain is shown in Fig. 6(b). Considering Fig. 6(b) the voltage stress of S in the proposed converter is less than the others except for one which presented in [11]. However, there is no considerable difference. As it is shown, voltage stress of S' is more than the others for a given specific voltage gain. But it should be considered that for this amount of voltage gain, the duty cycle of the proposed converter is less than the others. The value of the maximum current of switches demonstrated the merit of the lower duty cycle. The variation of maximum current of the switches versus voltage gain is shown in Fig. 6(c). As it is shown, the maximum value of the current of the switches of proposed converter is less than the others. As a conclusion for investigating the current and the voltage stress of the switches, the proposed converter is significantly superior to those of the mentioned literature.

The efficiency of the converters is stated in Table V, these amounts are obtained under the same conditions: $r_L = r_C = 0.05\Omega$, $r_D = 0.05\Omega$, $r_S = 0.085$, and $V_i = 20V$. According to Table V, it is clear that the efficiency of the proposed converter is higher than the others, however, it is lower than the conventional converter. It should be mentioned that the voltage gain of the conventional boost is not comparable with the proposed converter. Fig. 6(d) shows the variations of the efficiency versus the output power for $n = 1$,

$n=2$ and the amounts mentioned earlier. As it is shown in Fig. 7 the efficiency decreases as the output power increases. Furthermore, it decreases, for the same load, as the number of the switches and the inductors increase. It is due to the increase in series elements.

The cost of converters can be compared with their voltage and current stress on the semiconductors. If the current and voltage stress on each semiconductor multiply together and add them, an equation will be achieved. By this equation (here called S), the cost can be compared. In Fig. 7(a), the value of S is compared between some converters. As shown in Fig. 7(a), the normalized value of S based on output power for the proposed converter is lower than the converter in [11]. As can be seen, the value of the per united blocked power by the semiconductors for the proposed converter is higher than one in [10]. Variation of the normalized power of the inductors versus voltage gain is shown in Fig. 7(b). As can be seen the power of the proposed converter's inductors is lower than the presented converter in [10]. Although the blocked power by semiconductors for proposed converter is higher than one in [10] but the power of inductors is low. Considering Fig. 7 it can be concluded that the cost of the proposed converter is lower than the others.

VIII. Design of the Proposed Converter

In order to have a suitable operation, the elements of the converter should be designed optimally. In this paper, designing of the converter is done based on the OVR. Design of the elements of the proposed converter follows the presented procedure in [23-24]. It is assumed that $V_{i,\min} < V_i < V_{i,\max}$ and $R_{\min} < R < R_{\max}$. As it is comprehensible from (16) and (17), L_C and L_K are functions of V_i and R. For a specific inductance, the converter can operate in one of the operational modes while the input voltage and load resistance values vary.

The minimum and maximum critical inductances are given by applying the minimum and maximum value of V_i and R in (16) and (17). Classification of the modes and the operational regions versus the inductance values is shown in Table VI.

If the converter is designed for the worst conditions, it can operate well in normal condition. For the proposed converter the worst condition (maximum output voltage ripple (MOVR)) is in $(V_{i,\min}, R_{\min})$. Due to the different inductance values, the operational region of the proposed converter can be composed of five distinct sections on the inductance axis. Parameters $L_{K,\min}$ and $L_{C,\max}$ are significantly related to V_i and R. Therefore, the operation region classification would differ considering $L_{C\max} < L_{K,\min}$ or $L_{C\max} > L_{K,\min}$ conditions. The relation between MOVR in the operational region of the proposed converter is given in Table VII.

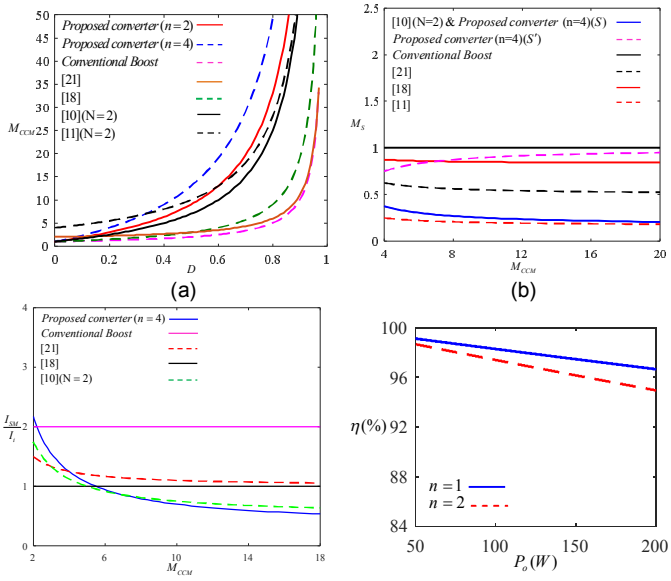


Fig. 6. Variation of (a) voltage gain versus duty cycle (b) voltage stress of the switches versus voltage gain. (c) Maximum current of the switches. versus voltage gain. (d). efficiency versus output power

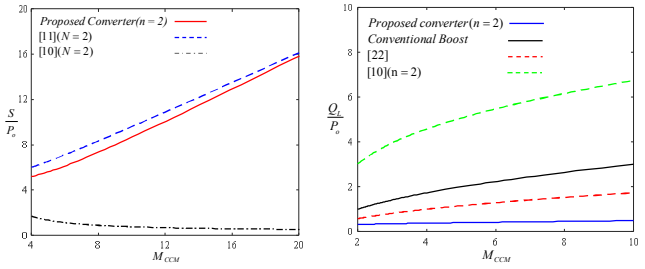


Fig. 7. Variation of (a) blocked power by semiconductors (b) power of the inductors versus voltage gain.

Variation of the output voltage ripple versus voltage gain is shown in Fig. 8. As can be seen, OVR of the proposed converter is minimum. Because of low voltage in renewable energy sources, high step up dc-dc converters are used to increase the voltage of these sources. On other hand the output of a high step up dc-dc converter is connected to the load to provide the energy of the load. In this condition quality of the waveform of the converter is a main issue. The proposed converter with minimum OVR can be used in these applications. Considering table 2 the efficiency of the proposed converter is higher than the others. The waveform of the input current is continuous and there is no need to design the filter in input, therefore it can be concluded that a proposed converter can be used in renewable energy sources.

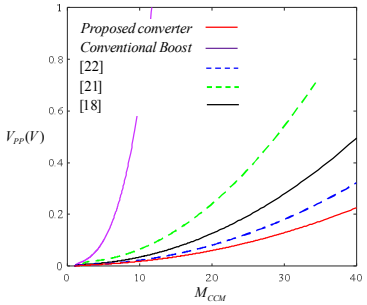


Fig. 8. Variation of the normalized OVR versus voltage gain

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TABLE V
PERFORMANCE BETWEEN DIFFERENT CONVERTERS

Converter	Conventional	[21]	[18]	[10]	[11]	Proposed
Switches	1	2	1	2	1	$n+2$
Diodes	1	1	3	2	4	$5n+6$
Inductors	1	1	2	4	2	$2n+4$
Voltage gain	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{2-D}{1-D}$	$\frac{1+(2N+1)D}{1-D}$	$\frac{2+N+ND}{1-D}$	$\frac{1+(2n+3)D}{1-D}$
Voltage stress of the switches	V_o	$\frac{V_o(1+M)}{2M}$	$\frac{V_o(M-1)}{M}$	$\frac{V_o[(2N+1)+M]}{(2N+2)M}$	$\frac{M+N}{2(N+1)M}$	$\frac{V_o[(n+1)+M]}{(n+2)M}$
Summation of Voltage stress of the switches	V_o	$\frac{V_o(1+M)}{M}$	$\frac{V_o(1+M)}{2M}$	$\frac{V_o[(2N+1)+M]}{(N+1)M}$	$\frac{M+N}{2(N+1)M}$	$\frac{V_o[(n+2)(1+M)]+\sum_{j=1}^{n}[(n-j+2)+jM)]}{(n+2)M}$
Voltage stress of the output diode	V_o	$\frac{V_o(1+M)}{M}$	$\frac{V_o(M-1)}{M}$	$\frac{V_o(1+2N)[(2N+1)+M]}{(2N+2)M}$	$\frac{(N+1)(M+N)}{2M(N+1)}$	$\frac{V_o(1+M)}{M}$
The maximum current through the switches	$2I_i$	$\frac{I_i(1+M)}{M}$	I_i	$\frac{I_i(1+N)(2N+M+1)}{(2N+2)M}$	$\frac{I_iM(N+1)(M+N)(N+2)}{2(N+1)^2}$	$\frac{I_i(n+1+M)}{(n+2)M}$
Efficiency $P_{out}=200W$	%98.33	%98.89	%90.5	%93.8	%93.9	%95.6

IX. Design Consideration

The design of the proposed converter is based on the least OVR and filter size. Considering Table III, if the converter operates in CISM-CCM, the OVR will be at its lowest value. According to Table VI, the inductance value should be higher than $L_{K,\max}$ in order to have the converter operate in CISM-CCM, however, this is not desirable due to the filter size. Therefore, $L<L_{K,\max}$. If $L<L_{C,\min}$, the converter will operate in IISM-DCM. Nevertheless, as it was mentioned previously, the OVR has the highest value in this mode. Therefore $L>L_{C,\min}$.It can be concluded that $L_{C,\min}<L<L_{K,\max}$.

It is obvious from Table VII that for $L>L_{K,\min}$ the OVR is independent of the inductance in CCM. For the least value of R and V_i, the minimum inductance value $L_{K,\min}$ is selected in order to ensure the occurrence of the minimum OVR.

According to Table III, MOVR is as follows:

$$V_{PP,\max}=\frac{V_o(V_o-V_{i,\min})}{fR_{\min}C[V_o+(2n+3)V_{i,\min}]} \tag{21}$$

The minimum value of output capacitor is as follows:

$$C_{\min}=\frac{V_o(V_o-V_{i,\min})}{fR_{\min}V_{PP,\max}[V_o+(2n+3)V_{i,\min}]} \tag{22}$$

TABLE VI
DIFFERENT OPERATIONAL MODES IN THE PROPOSED CONVERTER VERSUS INDUCTANCE VALUES

State	Operational mode	
$L>L_{C,\max}$	CCM	
$L<L_{C,\min}$	DCM	
$L_{C,\min}<L<L_{C,\max}$	$L>L_C$	CCM
	$L<L_C$	DCM
$L>L_{K,\max}$	CISM	

$L<L_{K,\min}$	IISM	
$L_{K,\min}<L<L_{K,\max}$	$L>L_K$	CISM
	$L<L_K$	IISM

TABLE VII
RELATION BETWEEN MOVRs

$L_{C\max}<L_{K,\min}$	$V_{PP1,\max}>V_{PP2,\max}>V_{PP3,\max}>V_{PP4,\max}=V_{PP5,\max}$
$L_{C\max}>L_{K,\min}$	$V_{PP1,\max}>V_{PP2,\max}>V_{PP3,\max}=V_{PP4,\max}=V_{PP5,\max}$

X. Control Strategy

Fig. 9 shows the diagram of the control strategy for the proposed converter. PWM (Pulse Width Modulation) method is used to control the switches. All of the switches turn on and off at the same time and they have the same duty cycle. In order to control the output voltage, a PI controller is used. The output voltage of the proposed converter is compared with the desired amount of the output voltage ($V_{o,ref}$) and if there is a difference it is applied to the controller to produce a desirable duty ratio. The desirable duty ratio is compared with a carrier wave, and then suitable interpolated pulses are produced to the switches. The PI controller has a gain and time constant that the amount of them is obtained by a trade-off.

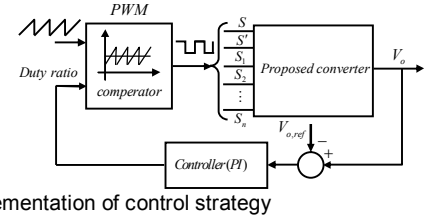


Fig. 9. Implementation of control strategy

XI. Experimental Results

In this section, experimental results are given to validate the performance of the proposed converter when $n=2$. Fig. 10 shows the photo of the hardware setup. The circuit component

values and their types are listed in Table VIII. By considering (14) and (15), for the given input voltage and load resistance values of $V_i = 30V$ and $R = 300\Omega$, the critical inductance values are obtained $L_C = 0.64mH$ and $L_K = 1.8\,mH$.

Fig. 11 shows the experimental and simulation results for $V_{\mathrm{i,min}} = 20V$ and $R_{\min} = 150\,\Omega$ (the MOVR conditions). As it is shown, if $L = 700\mu H$ is selected, the MOVR equals $3.07V$ owing to $L > L_{K,\min}$ .According to Fig. 11, it is also obvious that for $L = 800\mu H$ the maximum output voltage equals $3.07V$. Therefore, it can be concluded that for $L > L_{K,\min}$, the maximum output voltage ripple does not depend on the inductance value.

Fig. 12 shows the waveform of the voltage across the switches and output diode. for $L = 900\,\mu H$ .As shown in Fig. 12, the switches S and S' have the least and the most values of the voltage stress. The value of the voltage gain is 5.33 from Fig.11. By applying this value in Table II, the voltage stress of the output diode is obtained as $190V$, which is $188.06V$ in Fig. 12. According to the obtained values and comparing them with the experimental results, it can be concluded that the experimental results verify the theoretical analysis. The waveform of the current through the switches and diodes is shown in Fig. 13. In order to verify the theoretical analysis in more details, the experimental and theoretical results have been obtained and shown in Table IX. In which, the experimental results verify the theoretical results.

The waveform of the output voltage of the proposed converter with transient state is shown in Fig. 14. As can be seen, the output voltage has a short transient state.

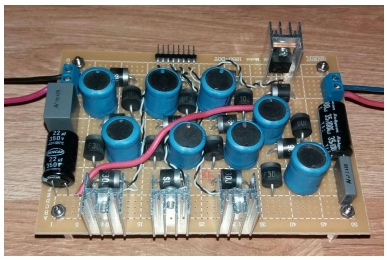
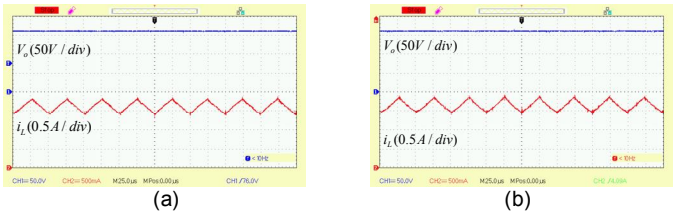


Fig. 10. Hardware setup of the proposed converter for $n = 2$

TABLE VIII
THE CONVERTER PARAMETERS

S_1, S_2, S, S'	$MOSFET\ IRF640$
$Diodes$	$SUF30$
V_o	$160V$
f	$20kHz$
R	$150-300\Omega$
C	$22\mu F / 350V$
$P_o(maximum\ output\ power)$	$200W$
V_i	$20-40V$



(a) (b)

Fig. 11. Experimental and simulation results in CCM for $V_{\mathrm{i,min}} = 20V$ and $R_{\min} = 150\,\Omega$. (a) $L = 700\mu H$. (b) $L = 800\mu H$.

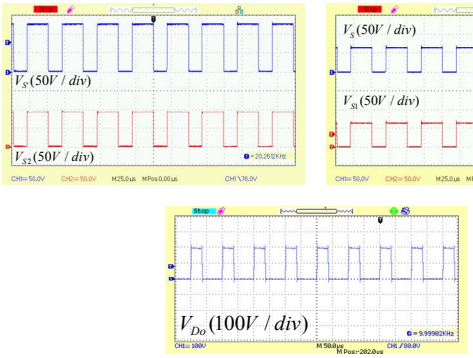


Fig. 12. Voltage stress of the switches and output diode in CCM for $L = 900\mu H$, $V_{\mathrm{i}} = 30V$ and $R = 300\,\Omega$

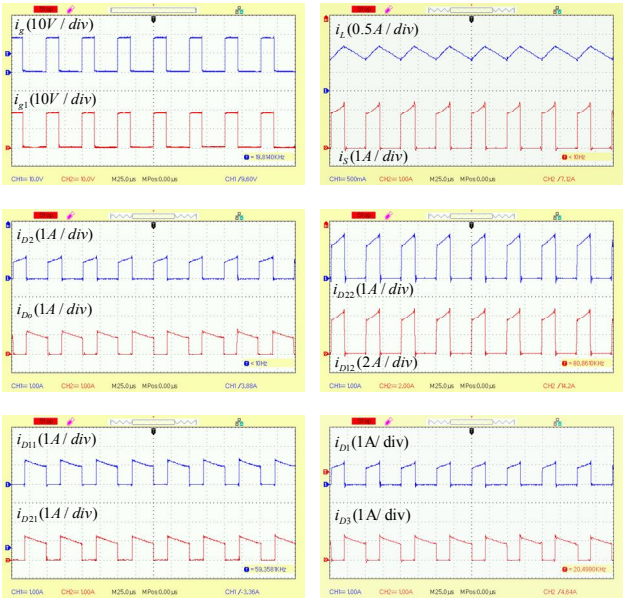


Fig. 13. Waveform of drive signals and current through the switches and diodes in CCM for $L = 900\mu H$, $V_{\mathrm{i}} = 30V$ and $R = 300\,\Omega$

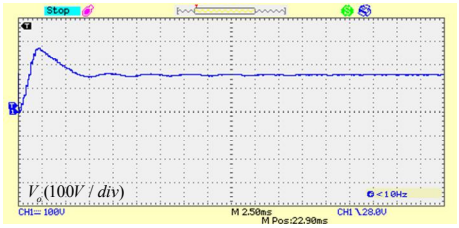


Fig. 14. The waveform of the output voltage with transient state

TABLE IX
COMPARISON BETWEEN EXPERIMENTAL AND THEORETICAL RESULTS

Parameters	Theoretical	Experimental

$V_{PP}(V)$	3.11	3.07
$I_{SP}(A)$	2.24	2.213
V_S	62.51	62.257
V_{S1}	62.51	62.257
V_{S2}	95	94.506
$V_{S'}$	127.5	126.755
V_{Do}	190.01	188.06
$V_{D1}=V_{D2}=V_{D13}=V_{D15}=V_{D23}=V_{D25}$	16.25	16.109
$V_{D3}=V_{D14}=V_{D24}=V_{D'3}$	30	29.86
$I_{D1P}=I_{D2P}=I_{D13P}=I_{D15P}=I_{D23P}=I_{D25P}$	1.12	1.107
$I_{D3P}=I_{D14P}=I_{D24P}=I_{D'3P}$	1.12	1.107
I_{D12P}	4.48	4.427
I_{D22P}	2.24	2.213
$I_{D11P}=I_{D21P}$	1.12	1.107

XII. Conclusion

A new, extendable high step-up dc-dc converter has been proposed. Extendibility of this converter is based on the APICs. The proposed converter can achieve a high gain with a small duty cycle which is difficult for the traditional boost converter. The voltage and current stress on semiconductor devices are low, which is beneficial to the system efficiency and cost. Because the switches are turned ON and OFF simultaneously, so one switching control circuit can be used. Suggested converter has been compared with presented structures in literature to mention the superiority. Considering the maximum output voltage ripple and filter size, an efficient method has been used to design the converter. The output voltage ripple is the least for $L = L_{K,\min}$ in CISM-CCM. The proposed converter is also flexible, which can adjust the quantity of APICs according to required gain. The experimental results have been given to verify the analysis and merits of the proposed converter.

References

[1] Y. Hu, W. Xiao, W. Cao, B. Ji, and D. J. Morrow, "Three-port dc-dc converter for stand-alone photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3068–3076, Jan. 2015.

[2] R.J. Wai, W.H. Wang, and C.Y. Lin, "High-performance stand-alone photovoltaic generation system," *IEEE Trans. Ind. Electron.,* vol. 55, no. 1, pp. 4278-4291, Jan. 2008.

[3] Y.P. Siwkoti, F. Blaabjerg, and P.C. Loh, "High step-up trans inverse dc-dc converter for the distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 316-322, March. 2016.

[4] H. Ardi, A. Ajami, and M. Sabahi, "A novel high step-up dc-dc converter with continuous input current integrating coupled inductor for renewable energy applications," *IEEE Trans. Ind. Electron,* in press (2017).

[5] W. Li, J. Liu, J. Wu, and X. He, "Design and analysis of isolated ZVT boost converters for high-efficiency and high-step-up applications," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2363–2374, Nov. 2007.

[6] C.M. Lai, Y.C. Lin, and Y.J. Lin, "Newly-constructed bidirectional dc-dc converter topology with high voltage conversion ratio for vehicle to dc-microgrid (V2DCG) system," in *Proc. IEEE 2nd International Future Energy Electronics Conference (IFEEC)* **,** 2015, pp. 1–8.

[7] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239- 1250 April 2011.

[8] G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3205–3214, Nov. 2011.

[9] M. Kim and S. Choi, "A fully soft-switched single switch isolated dc-dc converter**,"** *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4883–4890, Sept. 2015.

[10] L. Hong-Chen and L. Fei, "Novel high step-up dc-dc converter with active coupled-inductor network for a sustainable energy system," *IEEE Trans. Power Electron,* vol. 30, no. 12, pp. 6476–6482, Dec. 2015.

[11] J. Ai and M. Li, "Ultra-large gain step-up coupled inductor dc-dc converter with asymmetric voltage multiplier network for a sustainable energy system," *IEEE Trans. Power Electron,* vol. 32, no. 9, pp. 6896–6903, Sept. 2017.

[12] H. Wu, K, Sun, L. Chen, L. Zhu, and Y. Xing, "High step-up/step-down soft-switching bidirectional dc-dc converter with coupled-inductor and voltage matching control for energy storage systems," *IEEE Trans. Ind. Electron.,* vol. 63, no. 5, pp. 2892-2903, May 2016.

[13] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg "High-efficiency high step-up dc-dc converter with dual coupled inductors for grid-connected photovoltaic Systems," *IEEE Trans. Ind. Electron,* in press (2017).

[14] H. Mashinchi Maheri and E. Babaei, "Mathematical Modeling of buck-boost DC-DC converter and investigation of converter elements on transient and steady-state responses," *Int. J. Electr Power Energy Syst*, vol. 44, no. 1 pp. 949–963, Jan. 2013.

[15] D. Gunasekaran, L. Qin, Y. Karki, Y. Lin, and F.Z. Peng, "A variable (n/m)X switched capacitor dc-dc converter," *IEEE Trans. Power Electron.,* vol. 32, no. 8, pp. 6219–6235, Aug. 2017.

[16] S. Arslan, S. A. Ali Shah, J. J. Lee, and H. W. Kim, "An energy-efficient charging technique for switched capacitor voltage converters with low duty ratio," *IEEE Trans. Circuit and system-II.,* in press (2017).

[17] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687-696, Mar. 2008.

[18] E.H. Ismail, M.A. Al-Saffar, A.J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 4, pp. 1159–1171, May 2008.

[19] A.A. Fardoun, H.I. Esam, "Ultra step-up dc-dc converter with reduced switch stress", *IEEE Trans. Ind. Appl.,* vol. 46, no. 5 pp. 2025–2034, Sep./Oct. 2010.

[20] L. Schmitz, D. C. Martins, and R. F. Coelho, "Generalized high step-up dc-dc boost-based converter with gain cell," *IEEE Trans. circuits and systems-I,* vol. 64, no. 2, pp. 480–493, Feb. 2017.

[21] L.S. Yang, T.J. Liang, and J.F. Chen, "Transformerless dc-dc converters with high step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

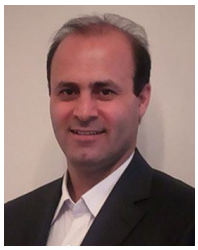
[22] Ki-Bum Park, Gun-Woo Moon, and Myung-Joong Youn, "Nonisolated high step-up boost converter integrated with sepic converter," *IEEE Trans. Power Electron,* vol. 25, no. 9, pp. 6476–6482, Sep. 2010.

[23] E. Babaei, M.E. Seyed Mahmoodieh, and H. Mashinchi Maheri "Operational modes and output voltage ripple analysis and design considerations of buck-boost dc-dc converters,". *IEEE Trans. on Ind. Electron.,* vol. 59, no. 1, pp. 381-391, Jan. 2012.

[24] H. Mashinchi, E. Babaei, S.H. Hosseini, and M. Sabahi, "High step-up dc-dc converter with minimum output voltage ripple," *IEEE Trans. Ind. Electron,* vol. 64, no. 5, pp. 3568–3575, May 2017.

[25] M.A.S. Masoum, H. Dehbonei, E.F. Fuchs, "Theoretical and experimentalanalyses of photovoltaic systems with voltage and current-based maximumpower-point tracking," *IEEE Trans. Energy Convers.* No. 4, vol. 17, pp. 514–522, Dec 2002.

[26] Y. C. Kuo and T. J. Liang, "Novel maximum-power-point-tracking controllerfor photovoltaic energy conversion system," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 594–601, Jul. 2001.



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