An Expandable Four-Phase Interleaved High Step-Down Converter with Low Switch Voltage Stress and Automatic Uniform Current Sharing

K. I. Hwu, *Member*, *IEEE*, W. Z. Jiang, *Student Member*, *IEEE*, and P. Y. Wu

***Abstract*—In this paper, a novel four-phase interleaved high step-down converter is presented. The proposed converter can provide an extremely high step-down voltage conversion ratio within a moderate duty cycle. There are four main advantages of the proposed converter. First, the blocking capacitors can store energy as usual. Therefore, they are used as voltage sources to reduce the input voltage as well as to reduce the switch voltage stresses. Second, due to the charge balance of the dc blocking capacitors, the converter possesses an automatic uniform current sharing characteristic of the interleaved phases without adopting any extra circuitry. Third, due to the phase shift between the interleaved phases, the architecture provides a low output current ripple. Fourth, the number of phases can be expanded or reduced to any even phases; therefore, the converter has a wide range of applications. Finally, the operating principles and analysis of this architecture are given, and an experimental prototype is also provided to verify the effectiveness of the proposed converter.**

***Index Terms*—High step-down converter, Automatic uniform current sharing, Low voltage stress, Interleaved control.**

I. INTRODUCTION

RECENTLY, a converter with high step-down voltage gain and large output current is increasingly needed, such as the battery charger, the power electronics used in the car, the distribution power system [2]-[4], and so on. Therefore, a high-performance buck converter is getting more and more attractive in the world. For applications possessing the non-isolated high step-down voltage gain and low output current ripple, the interleaved buck converter (IBC) [5]-[9] is widely used due to its simple structure and easy control.

However, since the traditional IBC has to endure a high input voltage, the high-voltage switch is required, and hence there are many disadvantages, such as high cost, large turn-on resistance, high turn-on driving voltage, large reverse recovery current, etc. For the applications of the high input voltage and extremely low output voltage, the duty cycle of the traditional buck converter will be extremely small, thereby leading to large power losses. Thus, the conversion efficiency of this buck converter would be reduced significantly.

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K. I. Hwu, W. Z. Jiang, and P. Y. Wu are with the Institute of Electrical Engineering, National Taipei University of Technology, Taipei 10608, Taiwan (e-mail: eaglehwu@ntut.edu.tw, newjerusalem333@gmail.com, and boyingwu77@gmail.com).

Consequently, in order to overcome the demerits mentioned above, there are many improved buck converter topologies presented [10]-[19]. The literatures [10] and [11] present high step-down converters based on switching capacitors, which are used as voltage dividers. By doing so, if the voltages across the capacitors are different, the output voltage would be deviated. In addition, too many switches and diodes are used, leading to efficiency reduction and cost increase. The literatures [12] and [13] present three-level step-down converters, which can reduce the voltage stresses across the switches from the input voltage to half of the input voltage. However, these two converters use too many components. The literature [14] presents a three-level high step-down buck converter with zero voltage switching (ZVS). Although this converter can provide a high step-down voltage gain, it uses two transformers, thereby causing the corresponding cost to increase and the indispensable leakage inductance energy to degrade the circuit efficiency regardless of ZVS operation. In literatures [15] and [16], not only the voltage stresses can be reduced by adjusting the turns ratio of the coupled inductor, but also a high step-down voltage gain can be obtained. In literature [17], an improved multiple-phase IBC is presented. This converter possesses a higher step-down voltage gain and lower voltages stresses on the switches than the traditional IBC. However, for high-input-voltage and low-output-voltage applications, the step-down voltage gain is not high enough. Consequently, an extremely small duty cycle is required to achieve a high step-down voltage gain, and this makes the overall efficiency low.

In order to obtain a reasonable duty cycle so as to upgrade the step-down voltage gain, the literatures [18] and [19] present multiphase IBCs with automatic current sharing and low voltage stresses on switches and diodes. Therefore, the corresponding conduction loss can be reduced and hence the overall efficiency can be improved. However, the input and output grounds are separated by the switches, thereby limiting converter applications as well as complicating control design. Moreover, the phase counts of the converters shown in [18] and [19] cannot be changed.

Based on the mentioned above, a novel four-phase high step-down converter with automatic current sharing and low voltage stresses on switches and diodes is proposed in this paper. Not only this converter can obtain a high step-down voltage gain under a suitable duty cycle, but also the input and output grounds are connected. In addition, the proposed

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converter possesses 2N (N is integer) multiphase extension capability. Furthermore, the output voltage ripple can be reduced by interleaved control.

II. Basic Operating Principles

Fig. 1 shows the four-phase step-down converter, which is constructed by four switches S_1, S_2, S_3 and S_4, four diodes D_1, D_2, D_3 and D_4, four inductors L_1, L_2, L_3 and L_4, three dc blocking capacitors C_1, C_2 and C_3, and one output capacitor C_o. Besides, the input voltage is represented by V_{in}, the output voltage is signified by V_o, and the output resistor is indicated by R_o. There are two functions of these dc blocking capacitors. One is that the high step-down voltage gain can be realized and the voltage stresses on switches and diodes can be reduced. The other is that the total output current can be evenly distributed among four phases. Fig. 2 shows the illustrated waveforms of the proposed converter operated in continuous conduction mode (CCM). It is noted that the automatic current sharing occurs under the condition that the duty cycle is smaller than 0.25 and the converter operates in CCM. If the number of phases is 2N, then the duty cycle is 0.5/N.

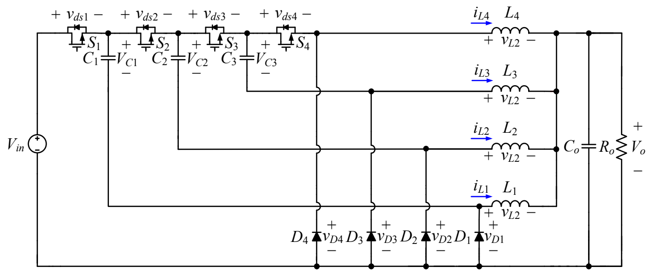

Fig. 1. Proposed expandable four-phase interleaved step-down converter.

For analysis convenience, there are some assumptions to be made as follows:

(1) All components used in this converter are ideal.

(2) The values of the capacitors C_1, C_2 and C_3 are identical and large enough to make the voltages across them kept constant without voltage ripples.

(3) The converter operates in CCM with the duty cycle D smaller than 0.25. Hence, not only the automatic current sharing among four phases but also the high step-down voltage conversion ratio can be achieved. In the proposed converter, there are eight operating modes.

1) State 1 $[t_0 \sim t_1]$*:* As shown in Fig. 3(a), during this interval, the switch S_1 is turned on, but the switches S_2, S_3 and S_4 are turned off. At the same time, the diode D_1 is turned off, but the diodes D_2, D_3 and D_4 are turned on. The input voltage V_{in} is across the capacitor C_1, the inductor L_1 and the output load, thus making C_1 being charged and L_1 being magnetized. Also, the currents i_{L2}, i_{L3} and i_{L4} are freewheeling via D_2, D_3 and D_4, respectively, thereby making the inductors L_2, L_3 and L_4 being demagnetized. Therefore, the voltage on D_1, v_{D1}, is clamped at $V_{in}-V_{C1}$, the voltage on S_2, v_{S2}, is clamped at $V_{in}-V_{C2}$, the voltage on S_3, v_{S3}, is clamped at $V_{C2}-V_{C3}$, and the voltage on S_4, v_{S4}, is clamped at V_{C3}. The associated differential equations are described below:

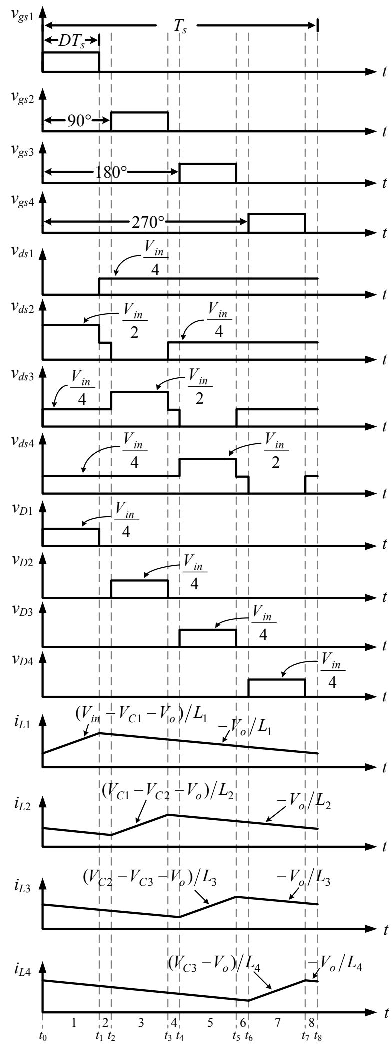

Fig. 2. Illustrated waveforms of the proposed converter operated in CCM.

$$L_1\frac{di_{L1}}{dt}=V_{in}-V_{C1}-V_o \quad (1)$$

$$L_2\frac{di_{L2}}{dt}=-V_o \quad (2)$$

$$L_3\frac{di_{L3}}{dt}=-V_o \quad (3)$$

$$L_4\frac{di_{L4}}{dt}=-V_o \quad (4)$$

$$C_1\frac{dv_{C1}}{dt}=i_{L1} \quad (5)$$

$$C_2\frac{dv_{C2}}{dt}=0 \quad (6)$$

$$C_3\frac{dv_{C3}}{dt}=0 \quad (7)$$

2) States 2, 4, 6, 8 $[t_1 \sim t_2,\ t_3 \sim t_4,\ t_5 \sim t_6,\ t_7 \sim t_8]$*:* As shown in Fig. 3(b), during these intervals, the switches S_1, S_2, S_3 and S_4 are all turned off. At the same time, the currents i_{L1}, i_{L2}, i_{L3} and i_{L4} are freewheeling via the diodes D_1, D_2, D_3 and D_4, respectively, thereby causing L_1, L_2, L_3 and L_4 to be demagnetized. Therefore, the voltage across S_1 is $V_{in} - V_{C1}$, the voltage across S_2, v_{S2}, is $V_{C1} - V_{C2}$, the voltage across S_3, v_{S3}, is $V_{C2} - V_{C3}$ and the voltage across S_4, v_{S4}, is V_{C3}.

$$L_1 \frac{di_{L1}}{dt} = -V_o \tag{8}$$

$$L_2 \frac{di_{L2}}{dt} = -V_o \tag{9}$$

$$L_3 \frac{di_{L3}}{dt} = -V_o \tag{10}$$

$$L_4 \frac{di_{L4}}{dt} = -V_o \tag{11}$$

3) State 3 $[t_2 \sim t_3]$*:* As shown in Fig. 3(c), during this interval, the switch S_2 is turned on, but the switches S_1, S_3 and S_4 are turned off. At the same time, the diode D_2 is turned off, but the diodes D_1, D_3 and D_4 are turned on. Also, the capacitor C_1 is releasing the energy to the capacitor C_2, the inductor L_2 and the load, thus making C_2 being charged and L_2 being magnetized. Besides, the currents i_{L1}, i_{L3} and i_{L4} are freewheeling via D_1, D_2 and D_4, thereby rendering the inductors L_1, L_3 and L_4 being demagnetized. Therefore, the voltage across D_2, v_{D2}, is $V_{C1} - V_{C2}$, the voltage across S_1, v_{S1}, is $V_{in} - V_{C1}$, the voltage across S_3, v_{S3}, is $V_{C1} - V_{C3}$ and the voltage across S_4, v_{S4}, is V_{C3}.

$$L_1 \frac{di_{L1}}{dt} = -V_o \tag{12}$$

$$L_2 \frac{di_{L2}}{dt} = V_{C1} - V_{C2} - V_o \tag{13}$$

$$L_3 \frac{di_{L3}}{dt} = -V_o \tag{14}$$

$$L_4 \frac{di_{L4}}{dt} = -V_o \tag{15}$$

$$C_1 \frac{dv_{C1}}{dt} = -i_{L2} \tag{16}$$

$$C_2 \frac{dv_{C2}}{dt} = i_{L2} \tag{17}$$

$$C_3 \frac{dv_{C3}}{dt} = 0 \tag{18}$$

4) State 5 $[t_4 \sim t_5]$*:* As shown in Fig. 3(d), during this interval, the switch S_3 is turned off, but the switches S_1, S_2 and S_4 are turned on. At the same time, the diode D_3 is turned off, but the diodes D_1, D_2 and D_4 are turned on. Also, the capacitor C_2 releases the energy to the capacitor C_3, the inductor L_3 and the load, thereby making C_3 being charged and L_3 being magnetized. Moreover, the currents i_{L1}, i_{L2} and i_{L4} are freewheeling via D_1, D_2 and D_4, respectively, thus making L_1, L_2 and L_4 being demagnetized. Therefore, the voltage across S_2, v_{S2}, is $V_{C1} - V_{C2}$ and the voltage across D_3, v_{D3}, is V_{C2}.

$$L_1 \frac{di_{L1}}{dt} = -V_o \tag{19}$$

$$L_2 \frac{di_{L2}}{dt} = -V_o \tag{20}$$

$$L_3 \frac{di_{L3}}{dt} = V_{C2} - V_{C3} - V_o \tag{21}$$

$$L_4 \frac{di_{L4}}{dt} = -V_o \tag{22}$$

$$C_1 \frac{dv_{C1}}{dt} = 0 \tag{23}$$

$$C_2 \frac{dv_{C2}}{dt} = -i_{L3} \tag{24}$$

$$C_3 \frac{dv_{C3}}{dt} = i_{L3} \tag{25}$$

5) State 7 $[t_6 \sim t_7]$*:* As shown in Fig. 3(e), during this interval, the switch S_4 is turned on, but the switches S_1, S_2 and S_3 are turned off. At the same time, the diode D_4 is turned off, but the diodes D_1, D_2 and D_3 are turned on. The capacitor C_3 releases energy to the inductor L_4 and the load, thus making L_4 magnetized. Also, the currents i_{L1}, i_{L2} and i_{L3} are freewheeling via D_1, D_2 and D_3, respectively, thereby rendering the inductors L_1, L_2 and L_3 being demagnetized. Therefore, the voltage across D_4 is $V_{L1} + V_o$, the voltage across S_1 is $V_{C1} - V_{C2}$, the voltage across S_2 is $V_{C1} - V_{C2}$ and the voltage across S_3 is $V_{C2} - V_{C3}$.

$$L_1 \frac{di_{L1}}{dt} = -V_o \tag{26}$$

$$L_2 \frac{di_{L2}}{dt} = -V_o \tag{27}$$

$$L_3 \frac{di_{L3}}{dt} = -V_o \tag{28}$$

$$L_4 \frac{di_{L4}}{dt} = V_{C3} - V_o \tag{29}$$

$$C_1 \frac{dv_{C1}}{dt} = 0 \tag{30}$$

$$C_2 \frac{dv_{C2}}{dt} = 0 \tag{31}$$

$$C_3 \frac{dv_{C3}}{dt} = -i_{L4} \tag{32}$$

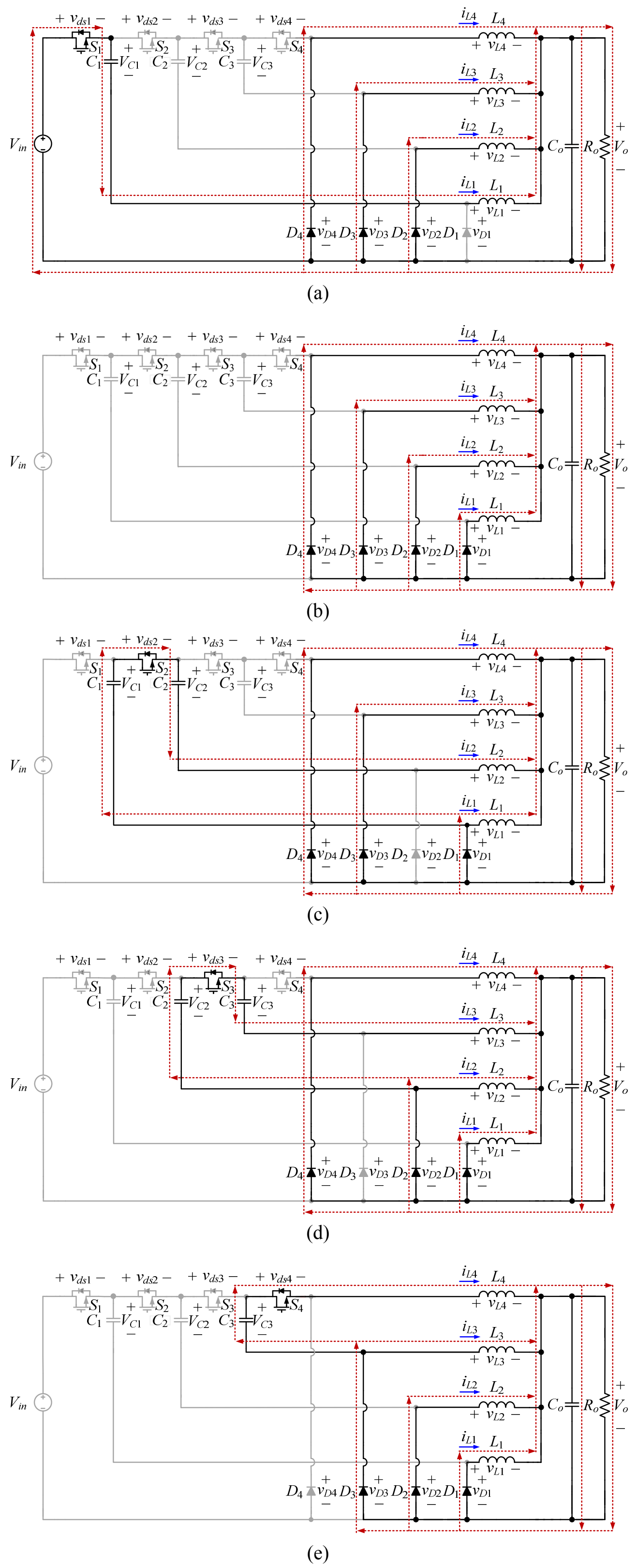

Fig. 3. Operating circuits over one switching period: (a) state 1; (b) state 2, 4, 6, 8; (c) state 3; (d) state 5; (e) state 7.

III. Steady State Analysis

A. Voltage Gain

Applying the volt-second balance to L_1, L_2, L_3 and L_4, the following equations can be obtained to be

$$(V_{in} - V_{C1} - V_o)D = V_o(1-D) \tag{33}$$

$$(V_{C1} - V_{C2} - V_o)D = V_o(1-D) \tag{34}$$

$$(V_{C2} - V_{C3} - V_o)D = V_o(1-D) \tag{35}$$

$$(V_{C3} - V_o)D = V_o(1-D) \tag{36}$$

Hence, the relationship between the output voltage V_o and the input voltage V_{in} can be described as follows:

$$V_o = \frac{D}{4} V_{in} \tag{37}$$

Accordingly, the voltage gain M can be obtained to be

$$M = \frac{V_o}{V_{in}} = \frac{D}{4} \tag{38}$$

B. Voltage Stresses on Switches and Diodes

According to Figs. 3(a), 3(c), 3(d) and 3(e), the voltages across D_1, D_2, D_3 and D_4 can be obtained to be

$$v_{D1} = V_{in} - V_{C1} \tag{39}$$

$$v_{D2} = V_{C1} - V_{C2} \tag{40}$$

$$v_{D3} = V_{C2} - V_{C3} \tag{41}$$

$$v_{D4} = V_{C3} \tag{42}$$

By substituting (37) into (33), (34), (35) and (36), the voltage across C_1, C_2 and C_3 can be obtained to be

$$V_{C1} = \frac{3}{4} V_{in} \tag{43}$$

$$V_{C2} = \frac{1}{2} V_{in} \tag{44}$$

$$V_{C3} = \frac{1}{4} V_{in} \tag{45}$$

Therefore, the voltage stresses on D_1, D_2, D_3 and D_4 can be obtained to be

$$v_{D1,max} = v_{D2,max} = v_{D3,max} = v_{D4,max} = \frac{V_{in}}{4} \tag{46}$$

According to Fig. 3(a), 3(c), 3(d) and 3(e), the voltages across the switches S_1, S_2, S_3 and S_4 are

$$v_{ds1} = V_{in} - V_{C1} \tag{47}$$

$$v_{ds2} = V_{in} - V_{C2} \tag{48}$$

$$v_{ds3} = V_{C1} - V_{C3} \tag{49}$$

$$v_{ds4} = V_{C2} \tag{50}$$

Therefore, the voltage stresses on these four switches can be obtained to be

$$v_{ds1,max} = \frac{V_{in}}{4} \tag{51}$$

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$$v_{ds2,max} = v_{ds3,max} = v_{ds4,max} = \frac{V_{in}}{2} \tag{52}$$

C. Auto Current Sharing

Based on (5), (16), (17), (24), (25) and (32) and by applying the ampere-second balance to the capacitors C_1, C_2 and C_3, the following equations can be obtained to be

$$\frac{I_{L1} - I_{L2}}{C_1} DT_s = 0 \tag{53}$$

$$\frac{I_{L2} - I_{L3}}{C_2} DT_s = 0 \tag{54}$$

$$\frac{I_{L3} - I_{L4}}{C_3} DT_s = 0 \tag{55}$$

Hence, the relationship between I_{L1}, I_{L2}, I_{L3} and I_{L4} can be expressed by

$$\begin{cases} I_{L1} - I_{L2} = 0 \\ I_{L2} - I_{L3} = 0 \\ I_{L3} - I_{L4} = 0 \end{cases} \tag{56}$$

The output current I_o can be signified by

$$I_{L1} + I_{L2} + I_{L3} + I_{L4} = I_o \tag{57}$$

From (56) and (57), the following equation can be obtained as

$$I_{L1} = I_{L2} = I_{L3} = I_{L4} = \frac{I_o}{4} \tag{58}$$

From (58), the current sharing can be achieved, independent of the values of the capacitors.

D. Boundary Condition and Inductor Design

1) Boundary Condition: What condition the inductors operate on is

$$\begin{cases} 2I_{Li} \geq \Delta i_{Li}, i = 1, 2, 3, 4 \Rightarrow \text{CCM} \\ 2I_{Li} < \Delta i_{Li}, i = 1, 2, 3, 4 \Rightarrow \text{DCM} \end{cases} \tag{59}$$

where I_{Li} and Δi_{Li} are the dc component of i_{Li} and the peak-to-peak value of the ac component of i_{Li}, i=1, 2, 3, 4, respectively.

Substituting (58) into (59) yields the following equation:

$$\begin{cases} I_o \geq 2\Delta i_{Li}, i = 1, 2, 3, 4 \Rightarrow \text{CCM} \\ I_o < 2\Delta i_{Li}, i = 1, 2, 3, 4 \Rightarrow \text{DCM} \end{cases} \tag{60}$$

From (60), if $I_o \geq 2\Delta i_{Li}$, then the converter operates in CCM; otherwise, the converter operates in discontinuous conduction mode (DCM).

2) Inductor Design: The system specifications are given in Table I. Based on Table I and (60), the value of the inductor of each phase for the proposed converter always operating in CCM should satisfy

$$L_i \geq \frac{V_o(1-D)T_s}{\Delta i_L} = \frac{24 \times (1-0.24) \times 25\mu}{2.083} = 218.9\ \mu\text{H}, i = 1, 2, 3, 4 \tag{61}$$

Finally, the value of L_i is set at $220\mu\text{H}$. Also, Table II shows the specifications of the components used for the proposed converter.

TABLE I
SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Input voltage (V_{in})	400V
Rated output voltage (V_o)	24V
Rated output current ($I_{o,rated}$) /power ($P_{o,rated}$)	20.83A/500W
Minimum output current ($I_{o,min}$)/power ($P_{o,min}$)	4.17A/100W
Switching frequency (f_s)	40kHz

TABLE II
COMPONENTS USED IN THE PROPOSED CONVERTER

Components		Specifications
Inductors L_1, L_2, L_3, L_4		220 μH
Capacitors C_1, C_2, C_3		10μF/450V
Output capacitor C_o		220μF/50V
Switches	S_1	IRFB4227PbF, 200V, $R_{ds(on)}$= 19.7mΩ
	S_2, S_3, S_4	IRFB4137PbF, 300V, $R_{ds(on)}$= 56mΩ
Diodes D_1, D_2, D_3, D_4		V40120C

E. Loss Analysis

Table III shows the voltage stresses on the switches and diodes of the classical interleaved buck converter (IBC), the converter in [19] and the proposed converter, whereas Table IV shows the MOSFET and diode specifications for the classical IBC, the converter in [19] and the proposed converter. Accordingly, under the specifications (400V input voltage, 24V output voltage, 500W output power, and 40kHz switching frequency), a loss breakdown comparison of between these three converters operating at rated load is made, and shown in Fig. 4.

TABLE III
COMPARISON OF THE STEADY-STATE CHARACTERISTICS ALONG WITH THE SELECTED PRODUCT NAMES

	Classical IBC		Converter in [19]		Proposed converter	
Duty ratio	1/16		1/4		1/4	
Voltage stress on switch	S_1	400V (IXFK64N50P)	S_2	100V (IXFH150N15P)	S_1	100V (IRFB4227PbF)
Voltage stress on switch	S_2	400V (IXFK64N50P)	S_1, S_3, S_4	200V (IXFH100N25P)	S_2, S_3, S_4	200V (IRFB4137PbF)
Voltage stress on diode	400V (DSEP 8-06A)		100V (DSSK 60-02A)		100V (V40120C)	

TABLE IV
PARAMETERS OF MOSFETS AND DIODES

MOSFET	Diode
IXFK64N50P, 500V, $R_{DS(on)}$=85mΩ	DSEP 8-06A, 600V, 10A, V_F=1.42V
IXFH150N15P, 150V, $R_{DS(on)}$=13mΩ	DSSK 60-02A, 200V, 60A, V_F=0.7V
IXFH100N25P, 250V, $R_{DS(on)}$= 27mΩ	
IRFB4227PbF, 200V, $R_{DS(on)}$=19.7mΩ	V40120C, 120V, 40A, V_F=0.63V
IRFB4137PbF, 300V, $R_{DS(on)}$=56mΩ	

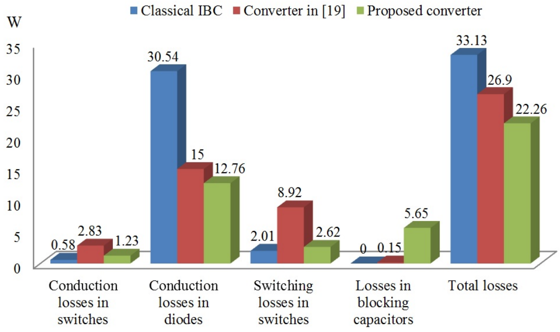

Fig. 4. Loss breakdown comparison.

IV. Experimental Results

In order to demonstrate the effectiveness of the proposed converter, the following waveforms are measured under the rated conditions. Fig. 5 shows the voltages v_{ds1}, v_{ds2}, v_{ds3} and v_{ds4} across the switches S_1, S_2, S_3 and S_4, respectively. From Fig. 5, it can be seen that the maximum values of v_{ds2}, v_{ds3} and v_{ds4} are 200V, equal to a half of the input voltage, which matches (52), and the maximum value of v_{ds1} is 100V, equal to a quarter of the input voltage, which matches (51).

Fig. 6 shows the voltages v_{ds1}, v_{ds2}, v_{ds3} and v_{ds4} across the diodes D_1, D_2, D_3 and D_4, respectively. From Fig. 6, it can be seen that the voltages v_{ds1}, v_{ds2}, v_{ds3} and v_{ds4} are 100V, equal to a quarter of the input voltage, which matches (46). Fig. 7 shows the voltages V_{C1}, V_{C2} and V_{C3} across the capacitors C_1, C_2 and C_3. From Fig. 7, the voltage across C_1 is 300V, equal to three-fourths of the input voltage, which matches (43); the voltage across C_2 is 200V, equal to a half of the input voltage, which matches (44); the voltage across C_3 is 100V, equal to a quarter of the input voltage, which matches (45).

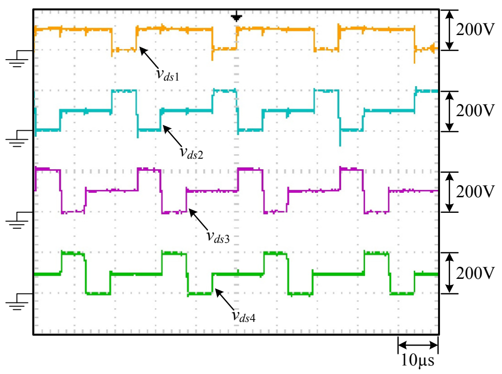

Fig. 5. Waveforms at rated load: (1) v_{ds1}; (2) v_{ds2}; (3) v_{ds3}; (4) v_{ds4}.

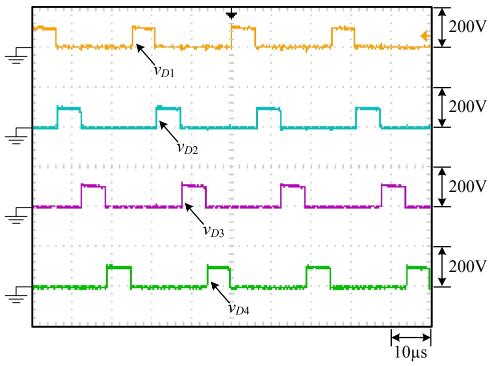

Fig. 6. Waveforms at rated load: (1) v_{D1}; (2) v_{D2}; (3) v_{D3}; (4) v_{D4}.

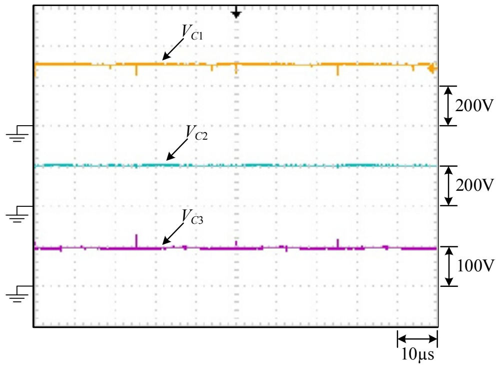

Fig. 7. Waveforms at rated load: (1)V_{C1}; (2) V_{C2}; (3) V_{C3}.

Figs. 8 and 9 show the currents i_{L1}, i_{L2}, i_{L3} and i_{L4} in L_1, L_2, L_3 and L_4, respectively. From Fig. 9, it can be seen that the output current is evenly distributed among four phases. Fig. 10 shows the input voltage V_{in} and the output voltage V_o. From Fig. 10, it can be seen that the input voltage V_{in} is 400V and the output voltage V_o is 24V, and this verifies the high step-down voltage gain. Fig. 11 shows the curve of efficiency versus load current as compared to the literature [19]. From Fig. 11, it can be seen that the efficiency of the proposed converter is better than that of the converter in [19].

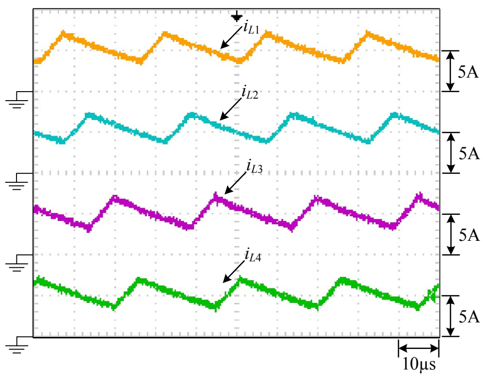

Fig. 8. Waveforms at rated load: (1) i_{L1}; (2) i_{L2}; (3) i_{L3}; (4) i_{L4}.

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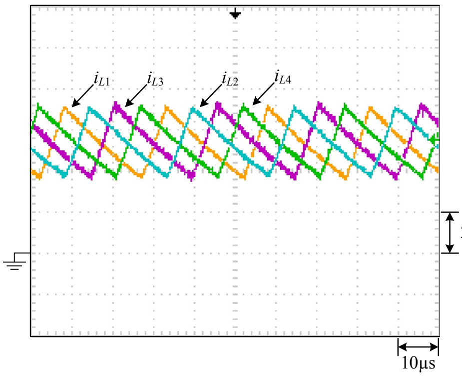


Fig. 9. Waveforms at rated load: (1) i_{L1}; (2) i_{L2}; (3) i_{L3}; (4) i_{L4}.

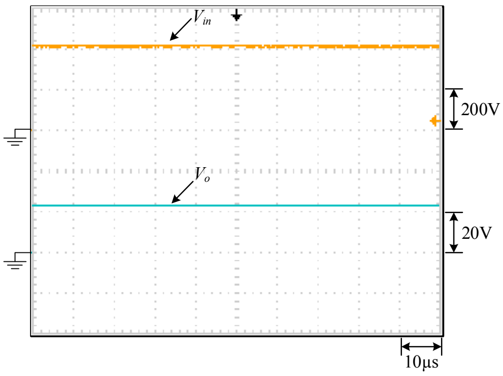


Fig. 10. Waveforms at rated load: (1) V_{in}; (2) V_o.

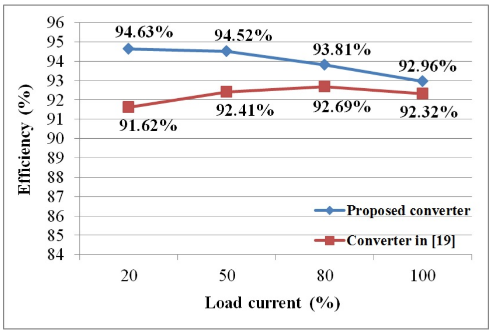


Fig. 11. Curves of efficiency versus load current as compared with the converter in [19].

Under the condition that the input voltage of the proposed converter is connected to the output voltage of the power supply, Figs. 12 to 14 show the input voltage and the voltages across the three dc blocking capacitors during the power-on and -off transitions. From these figures, all the voltages on these dc blocking capacitors almost linearly rise, synchronized with the input voltage with different slopes. Also, the voltages across all the switches during the power-on and -off transitions can be represented by (47) to (50). Based on (47) to (50) and Figs. 12 to 14, it can be seen that the voltage stresses on all the switches during the power-on and -off transitions are smaller than the input voltage.

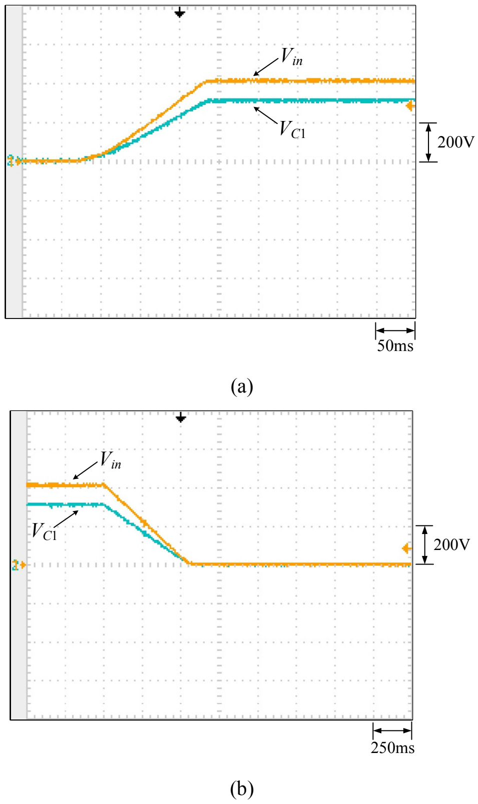


Fig. 12. Transitions of V_{in} and V_{C1}: (1) power-on; (2) power-off.

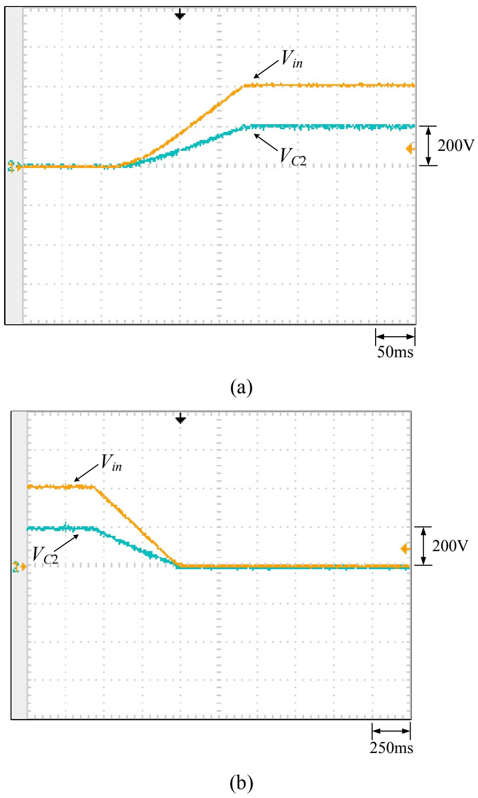
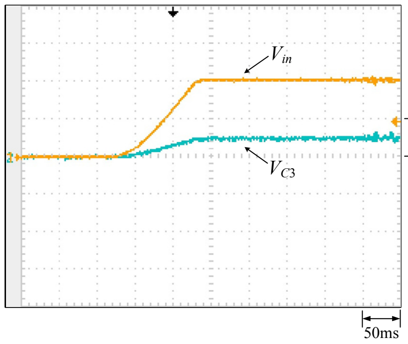
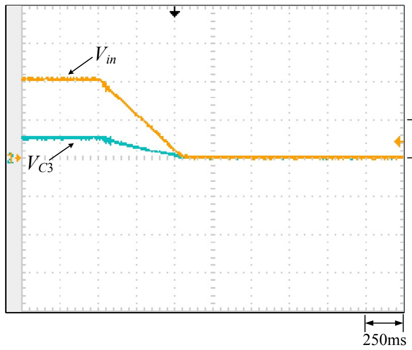


Fig. 13. Transitions of V_{in} and V_{C2}: (1) power-on; (2) power-off.



(a)



(b)

Fig. 14. Transitions of V_{in} and V_{C3}: (1) power-on; (2) power-off.

V. Conclusion

In this paper, a novel four-phase interleaved converter is presented, which possesses a high step-down voltage gain and automatic current balance. Above all, the number of phases can be increased or decreased. Due to the dc blocking capacitors, the switches and diodes have relatively low voltage stresses, and hence the conduction and switching losses are reduced. Furthermore, unlike the converter shown in [19], the input and output grounds of the proposed converter are connected. Moreover, the associated mathematical deductions for the proposed converter are given first, and then some experimental results, based on a prototype with 400V input voltage, 24V output voltage and 500W output power, are used to verify the merits of the proposed converter. Accordingly, the experimental results show the low voltage stresses and the automatic uniform current sharing characteristic. In addition, the experimental results also show the relationship between the input voltage and the dc blocking capacitor voltages during power-on and power-off transitions. When the input voltage linearly rises during the startup period, these dc blocking capacitor voltages also linearly rise. When the input voltage linearly falls to zero during the shutdown period, these dc blocking capacitor voltages also linearly fall to zero. Thus, there are no over-voltages on the switches during power-on and power-off transitions.

The proposed converter can be used in the applications with high input voltage and low output voltage, such as battery chargers, distributed power systems, etc.

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K. I. Hwu (M'06) was born in Taichung, Taiwan, on August 24, 1965. He received the B.S. and Ph.D. degrees in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1995 and 2001, respectively.

From 2001 to 2002, he was the Team Leader of the Voltage-Regulated Module (VRM) at AcBel Company. From 2002 to 2004, he was a Researcher at the Energy and Resources Laboratories, Industrial Technology Research Institute. He is currently a Professor at the Institute of Electrical Engineering, National Taipei University of Technology, Taipei, Taiwan, where he was the Chairman of the Center for Power Electronics Technology from 2005 to 2006. His fields of research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.

Dr. Hwu has been a member of the Program Committee of the IEEE Applied Power Electronics Conference and Exposition since 2005. He has also been a member of the Technical Review Committee of the Bureau of Standards, Metrology, and Inspection since 2005. Since 2008, he has been a member of the IET.

W. Z. Jiang (S'12) was born in Changhua, Taiwan, on May 9, 1989. He received the B.S. and M.S. degrees in electrical engineering from National Taipei University of Technology, Taipei, Taiwan, in 2011 and 2013, respectively. Currently, he is working toward a Ph.D. degree at National Taipei University of Technology. His fields of research interests include converter topologies, magnetic component applications, power factor correction rectifiers, sustainable energy applications, LED lighting drivers, and digital control.

P. Y. Wu was born in Taipei, Taiwan, on July 7, 1992. He received the B.S. degree in electrical engineering from National Taipei University of Technology, Taipei, Taiwan, in 2014. Currently, he is working toward a M.S. degree at National Taipei University of Technology. His fields of research interests include power electronics and digital control.