A Time-Domain Resolution Improvement of an RF-DAC

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***Abstract*—We propose a time-domain technique that significantly improves resolution of an RF digital-to-analog converter (RF-DAC). As an alternative to resorting to various resolution improvement attempts in the amplitude domain or through quantization noise shaping, pulsewidth modulation (PWM) of a single least significant bit device is employed with fine timing accuracy easily afforded by advanced CMOS technology. The technique is examined in the context of a commercial Enhanced Data rates for GSM Evolution (EDGE) polar transmitter realized in 65-nm CMOS, which employs an amplitude modulator with basic 10-bit amplitude resolution limited by the RF-DAC switching device mismatches. Behavioral simulations include realistic device mismatches and show worst-case resolution improvement of 2.2 bits assuming 20-ps worst-case time granularity of the PWM signal controls.**

***Index Terms*—Amplitude modulation, polar transmitter, pulsewidth modulation (PWM), radio frequency digital-to-analog converter (RF-DAC).**

I. Introduction

NOWADAYS, most wireless applications require extensive digital functionality. Ideally, integrating RF circuits with digital logic is desired for lower cost, form factor, and power dissipation. Some RF transmitters presented in recent publications have suggested using an RF digital-to-analog converter (RF-DAC) for easier system-on-a-chip (SoC) implementation [1]–[4]. Among them, the commercial single-chip Global System for Mobile Communications (GSM)/Enhanced Data rates for GSM Evolution (EDGE) transceiver in [1] and [2] is unique in that it uses an array of unit-weighted transistor switches to control the output RF amplitude instead of using a traditional current-source-based digital-to-analog converter (DAC) structure.

Fig. 1 illustrates the polar transmitter introduced in [1] and [2]. The in-phase/quadrature baseband data are converted into amplitude and phase/frequency polar components. The frequency signal is fed into the digitally controlled oscillator (DCO)-based N_F-bit digital-to-frequency converter, which generates a digital phase-modulated RF carrier by means of an all-digital phase-locked loop (ADPLL). The amplitude signal drives the N_A-bit digital-to-RF-amplitude converter (DRAC), which includes a digitally controlled power amplifier (DPA). The amplitude of the output RF carrier signal is controlled by the number of engaged switching devices.

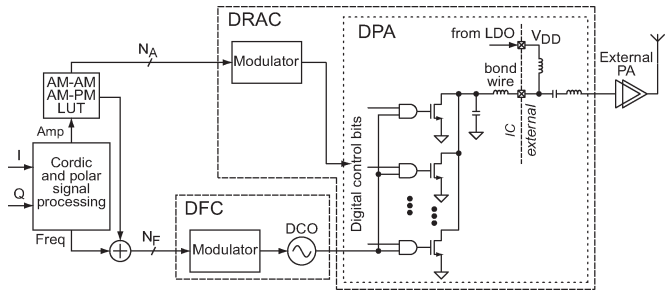

Fig. 1. Polar transmitter based on a DCO and DPA circuits. For simplicity, the ADPLL around the DCO is not shown.

The DRAC controls the envelope of the phase-modulated RF carrier, and thus, it is considered an RF-DAC. The main difference between the DRAC and the traditional RF-DAC in [3] or [4] is that the DRAC eliminates current sources to make it more compatible with low-voltage and low-cost digital CMOS processes. The lookup table (LUT) in the amplitude signal path shown in Fig. 1 is used for amplitude modulation/amplitude modulation and amplitude modulation/phase modulation predistortion to linearize the DPA transfer function.

The approach in [1] and [2] proved that the architecture in Fig. 1 is feasible for SoC, and it meets all GSM and EDGE specifications. However, the resolution of the amplitude path is limited by lithography and RF mismatches (i.e., both amplitude and phase) of the switching devices in the DPA, and consequently, the polar transmitter has little margin in the far-out (i.e., the associated receiving (RX) band) noise limit of the surface acoustic wave-less operation for EDGE. A $\Sigma\Delta$ dithering of the LSB device is used to improve the resolution, although it pushes the quantization noise to higher frequencies where emission requirements might sometimes be difficult to satisfy in a multiradio environment. In this brief, we address the far-out noise issue and make this architecture more attractive to advanced modulation standards, and we propose an RF-DAC structure in which significant resolution improvement is achieved by means of *incremental* pulsewidth modulation (PWM).

We first discuss the details of the PWM scheme to improve the amplitude resolution of the DPA. It will be shown that a straightforward PWM method creates an incorrect RF signal. Predistortion of PWM signals to generate a correct RF signal is then presented. Finally, behavioral simulation results are presented to show the benefits of the proposed method.

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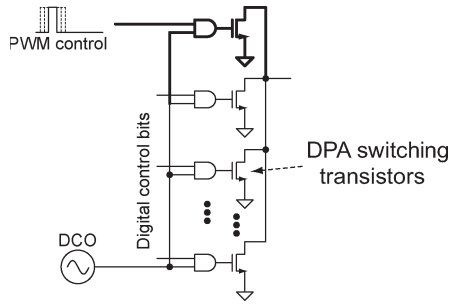

Fig. 2. Amplitude resolution improvement by adding a PWM-driven transistor.

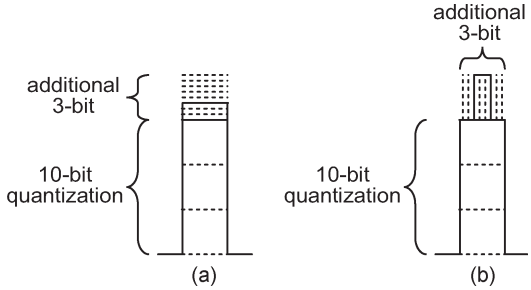

Fig. 3. Amplitude resolution improvement by (a) horizontal slicing (b) vertical slicing.

II. Resolution Enhancement Approaches Employing PWM

We propose that the original DPA from Fig. 1 simply be augmented by one additional switching device that is driven by a PWM signal, as shown in Fig. 2. The amplitude resolution of the DPA improves by turning on the switching devices for only a short time interval within the positive half-cycle of the RF period. The RF output amplitude will be controlled by the time interval, and the resolution is determined by the time precision of the turning-on signal. The amplitude resolution of the DPA in Fig. 2 is now limited by the time resolution of the PWM. In modern CMOS processes, the switching time gets improved by $0.7\times$ per node; hence, achieving higher resolution in the time domain is easier than in the voltage/current domain. In a 65-nm CMOS process, a minimum time resolution of 20 ps is easy to guarantee over process, temperature, and voltage variations.

The output amplitude of a PWM signal at the frequency of interest, however, is incorrect if the pulsewidth is chosen in a straightforward way such that the dc amplitude of the PWM signal is correct [5], [6]. This is in contrast with the normal upconversion operation of the DPA, which acts as a mixer. As a result, this inaccurate RF output level at the carrier frequency turns out to limit the resolution improvement.

To explain this issue, Fig. 3 illustrates two different quantization methods for adding an extra 3-bit resolution in either a voltage or a current signal. For the DPA, the vertical axis in Fig. 3 represents the current drawn by the switching transistors, which is directly proportional to the output envelope, and its original resolution is 10 bits in the system of Fig. 1. Fig. 3(a) shows *horizontal slicing* of a signal, which is a conventional quantization method for a DAC. Fig. 3(b) shows *vertical slicing* of a signal, where the output amplitude is controlled by the time interval of the vertically sliced signal. This quantization method is PWM, whose pulsewidth has a limited number of quantized pulsewidths.

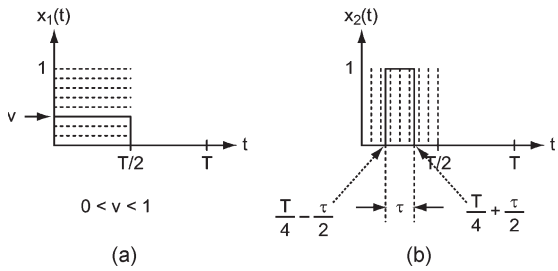

Fig. 4. (a) LSB portion of horizontal slicing. (b) LSB portion of vertical slicing.

For the horizontal slicing scheme, the resolution is set by available area and power, along with device mismatch, which limits the minimum device size. In contrast, the resolution of the vertical slicing scheme is set by time resolution. Accordingly, vertical slicing can achieve higher resolution than horizontal slicing with the same LSB device size if time resolution is higher. In modern nanoscale CMOS technology, time resolution is getting higher; thus, employing PWM is a better choice to improve the amplitude resolution of a DPA.

Fig. 4 illustrates only the LSB portions from Fig. 3, where T is the time period of an RF carrier signal, v is an LSB voltage/current level by horizontal slicing, and τ is a pulsewidth for vertical slicing. Note that the amplitude switches are only turned on during half the DCO period, i.e., $T/2$. The full size of this LSB is normalized to 1. The LSB adds an extra 3-bit resolution with eight extra amplitude levels. The pulse position of the PWM signal is assumed to be at the center of the first half-cycle of the carrier signal in this case.

Intuitively, both signals from Fig. 4(a) and (b) are the same in terms of power because the total areas of the signals are the same. As pointed out in [5], however, they are equivalent only at dc. The Fourier transforms of the horizontal and vertical slicing signals, respectively, are

$$X_1(j\omega) = \int_0^{\frac{T}{2}} v \cdot e^{-j\omega t} dt = v \cdot \frac{2e^{-j\frac{\omega T}{4}} \cdot \sin\left(\frac{\omega T}{4}\right)}{\omega}$$

$$X_2(j\omega) = \int_{\frac{T}{4}-\frac{\tau}{2}}^{\frac{T}{4}+\frac{\tau}{2}} e^{-j\omega t} dt = \frac{2e^{-j\frac{\omega T}{4}} \cdot \sin(\frac{\omega \tau}{2})}{\omega}.$$

In the examples of Fig. 4, v is 3/8, and τ is $(3/8) \times (T/2)$. Fig. 5 illustrates the amplitudes of the Fourier transforms of each case, and it clearly shows that horizontal and vertical slicing *are not the same* at the carrier frequency, which is $(1/T)$ Hz. An RF-DAC is intended to generate a signal at a carrier frequency corresponding to an input digital code. Therefore, the vertical slicing signal in Fig. 5 creates an incorrect RF signal, although it creates an accurate dc signal.

An inaccurate RF signal from an RF-DAC leads to higher quantization noise. The Fourier transforms at a carrier frequency $(\omega = 2\pi/T)$ should be looked at for quantization noise analysis for an RF-DAC, and they are

$$X_1(j\omega)|_{\omega=\frac{2\pi}{T}} = \frac{-jvT}{\pi} \quad (1)$$

$$X_2(j\omega)|_{\omega=\frac{2\pi}{T}} = \frac{-j\,\sin\left(\frac{\pi\tau}{T}\right)T}{\pi}. \quad (2)$$

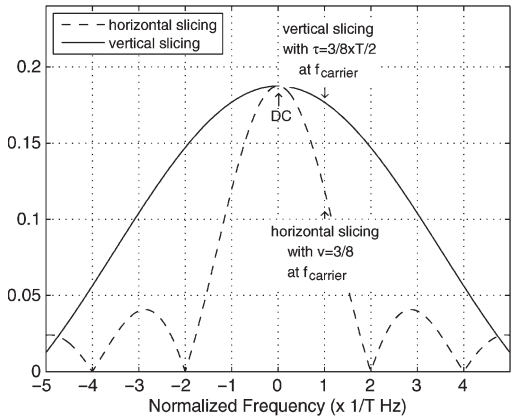

Fig. 5. Frequency-domain amplitude comparison of vertical slicing and horizontal slicing when $v = 3/8$ and $\tau = (3/8) \times (T/2)$.

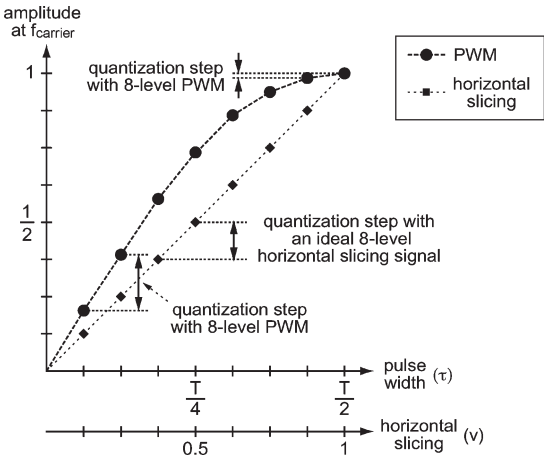

Fig. 6. Amplitude quantization step at the carrier frequency of horizontal slicing signals and eight-level PWM signals [6].

Fig. 6 depicts the amplitudes at the carrier frequency of the eight-level horizontal and vertical slicing signals, which are derived in (1) and (2) as a function of pulsewidth and horizontal slicing level. As shown in Fig. 6, the amplitude at the carrier frequency with vertical slicing is always bigger than what it should be. Because of the inaccurate amplitude, the calculated resolution of vertical slicing with an eight-level input code is only 0.9 bit, whereas horizontal slicing achieves 3-bit resolution. Therefore, resolution improvement by PWM is severely impaired if the pulsewidth is chosen in such a way that the dc amplitude of a vertical slicing signal is matched with that of a horizontal slicing signal, as shown in Fig. 6.

III. Predistortion of PWM Signals

One solution to the discrepancy between horizontal and vertical slicing is choosing the pulsewidth for vertical slicing such that its amplitude at the carrier frequency is the same as that of corresponding horizontal slicing.

Equation (3) shows how to choose the pulsewidth, i.e.,

$$\begin{aligned} X_1(j\omega)|_{\omega=\frac{2\pi}{T}} &= X_2(j\omega)|_{\omega=\frac{2\pi}{T}} \\ \frac{-jvT}{\pi} &= \frac{-j\,\sin\left(\frac{\pi\tau}{T}\right)T}{\pi} \\ v &= \sin\left(\frac{\pi\tau}{T}\right). \end{aligned} \tag{3}$$

TABLE I
Pulsewidths That Create the Same Amplitude at a Carrier Frequency as the Corresponding Horizontal Slicing Signals

horizontal slicing	pulse width	horizontal slicing	pulse width
0	0	$\frac{4}{8}$	$0.166667 \times T$
$\frac{1}{8}$	$0.039898 \times T$	$\frac{5}{8}$	$0.214901 \times T$
$\frac{2}{8}$	$0.080431 \times T$	$\frac{6}{8}$	$0.269947 \times T$
$\frac{3}{8}$	$0.122357 \times T$	$\frac{7}{8}$	$0.339139 \times T$

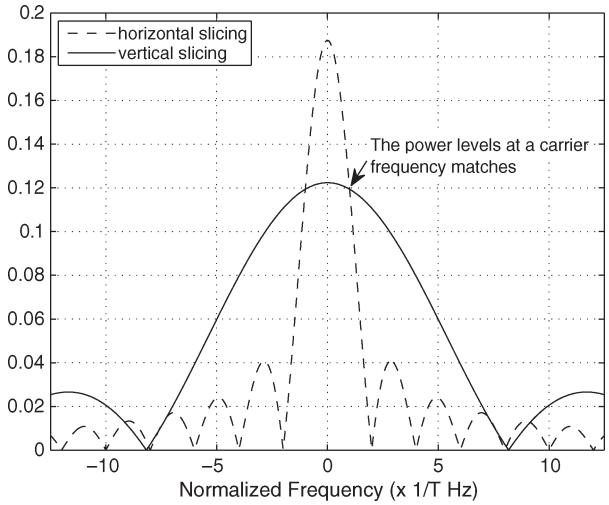

Fig. 7. Frequency-domain amplitude comparison of vertical slicing and horizontal slicing when $v = 3/8$ and $\tau = 0.122357 \times T$.

A PWM signal whose pulsewidth satisfies (3) has the same amplitude as the corresponding horizontal slicing signal at the carrier frequency.

The position of the PWM signal is assumed to be at the center of the turn-on period of other MSB switching devices, as depicted in Fig. 4(b). We will call this *centered PWM* to distinguish it from *noncentered PWM*. For centered PWM, according to (1) and (2), the phases of the Fourier transforms are the same; consequently, only the amplitude of the PWM signal at the carrier frequency needs to be considered.[1]

Table I shows an example of the pulsewidths for which the amplitude and the phase at the carrier frequency are the same as those of the corresponding horizontal slicing signals.

Fig. 7 depicts an example of the amplitudes of the Fourier transforms of vertical slicing signals satisfying (3), as shown in Table I. In Fig. 7, it is clear that the amplitude of the vertical slicing signal at the carrier frequency is the same as that of the horizontal slicing signal. As a result, the amplitude resolution of the PWM signals employing the pulsewidths shown in Table I is also the same as that of horizontal slicing signals. Unfortunately, the pulsewidths shown in Table I are very challenging to generate without an accurate delay controller, such as a high-precision delay-locked loop (DLL) or a fine-resolution delay line. Therefore, such PWM generation is impractical.

A PWM signal is easier to generate when its pulsewidth is integer multiples of a certain delay. Table II shows an example in which the pulsewidths are integer multiples of $T/16$. It also presents the corresponding horizontal slicing signals that

[1]In this brief, we do not further discuss the noncentered PWM. The noncentered PWM scheme will be covered in a future paper.

TABLE II
PULSEWIDTHS THAT ARE MULTIPLES OF $T/16$ AND EQUIVALENT HORIZONTAL SLICING SIGNALS

horizontal slicing	pulse width	horizontal slicing	pulse width
0	0	0.707107	$\frac{4}{8} \times \frac{T}{2}$
0.194090	$\frac{1}{8} \times \frac{T}{2}$	0.831470	$\frac{5}{8} \times \frac{T}{2}$
0.382683	$\frac{2}{8} \times \frac{T}{2}$	0.923880	$\frac{6}{8} \times \frac{T}{2}$
0.555570	$\frac{3}{8} \times \frac{T}{2}$	0.980785	$\frac{7}{8} \times \frac{T}{2}$

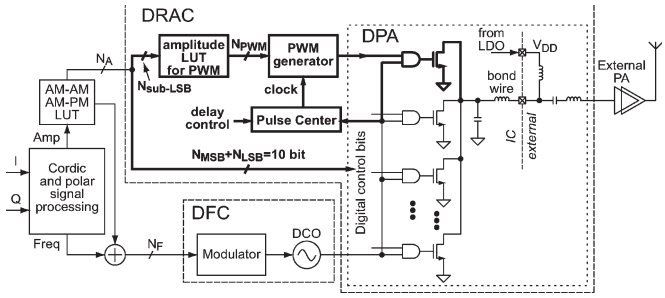

Fig. 8. Proposed polar transmitter with PWM.

satisfy (3). A simple delay chain can generate those pulsewidths shown in Table II; hence, it is a better implementation choice. However, the relationship between the desired horizontal slicing signals and the pulsewidths shown in Table II is nonlinear. A predistortion digital LUT can be utilized to implement this mapping, where the contents of the predistortion LUT should be chosen such that the amplitude quantization error is minimized.

The quantization error using a predistortion LUT and eight-level PWM will be larger than that of the ideal 3-bit horizontal slicing. The calculated amplitude resolution using the LUT with a 5-bit input code and an eight-level PWM output is 2.6 bits.

As shown in Tables I and II, there are two options to linearize the RF power of a PWM signal, i.e., mapping uniform data input to nonuniform pulsewidths (Table I) and mapping nonuniform data input to uniform pulsewidths (Table II). Apparently, uniform-to-nonuniform mapping needs no sacrifice for achieving 3-bit resolution, whereas nonuniform-to-uniform mapping shows resolution degradation by 0.4 bits. However, the pulsewidths in Table II are easy to generate using a simple delay chain. The predistortion LUT is also easy to implement in digital CMOS processes. Therefore, we propose to employ the PWM method using a predistortion LUT, which helps minimize the overall system complexity with a slight degradation of amplitude resolution.

IV. PROPOSED ARCHITECTURE EMPLOYING PWM

Fig. 8 illustrates the proposed architecture with a PWM generator. Note that the proposed architecture is augmented from the original polar transmitter architecture depicted in Fig. 1. The building blocks drawn with the bold lines are added to the original polar transmitter to improve its amplitude resolution. In Fig. 8, the PWM generator makes $2^{N_{\mathrm{PWM}}}$-level PWM signals. The original amplitude signal is N_A bits. The MSB/LSB signals from the original architecture are 10 bits, and they directly drive the DPA's switching transistors. The $N_{\text{sub-LSB}}$-bit sub-LSB signals go into the amplitude predistortion LUT for PWM, which is realized based on (3). The LUT has $N_{\text{sub-LSB}}$-bit inputs and N_{PWM}-bit outputs. It will occupy a very small area in modern CMOS processes because its size is only $2^{N_{\text{sub-LSB}}}$ words. In this brief, we used 5-bit sub-LSB signals as input and 12-level PWM signals as output, which are represented by 32 four-bit data words in the predistortion LUT. Therefore, the size of the required LUT for PWM is 2^5 words $\times$ 4 bits $=$ 128 bits. Note that this LUT can also be merged with the LUT for DPA in the original polar transmitter to minimize the area.

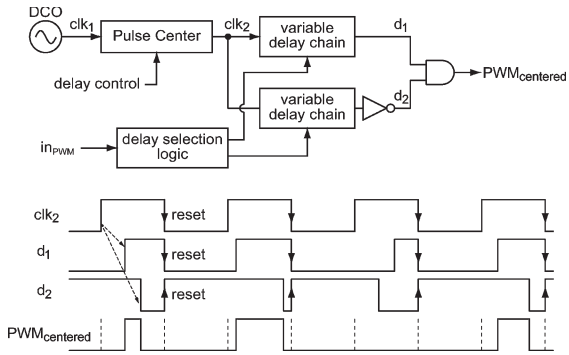

Fig. 9. Conceptual block diagram of a PWM generator and its timing diagram.

Fig. 9 depicts the conceptual block diagram of a centered PWM generator and an example of the timing diagrams. The key idea is to adjust two pulse signals, i.e., d_1 and d_2, with two simple delay chains to produce the desired pulse output.

To achieve better centering ability, a *Pulse Center* block in Figs. 8 and 9, which can be implemented with either a DLL or fine-resolution delay lines, manipulates the main clock delay, thereby controlling the pulse position of the PWM signal. The Pulse Center block plays an important role in that it keeps the position of the PWM at the center of the MSB transistor turn-on time, as depicted in Fig. 4(b), across process variation. If the PWM is not located at the center, it causes phase distortion of the output signal. Pulse centering using the Pulse Center block can compensate for the impact of process variation. Channel switching is another issue since the pulse position is relative to the clock period T. Therefore, the relative pulse position changes if the clock period is changed. The Pulse Center block can change the delay for the clock input of the PWM generator, i.e., clk_2, such that the pulse position is always centered no matter what transmission channel is selected.

V. BEHAVIORAL SIMULATIONS OF THE PROPOSED ARCHITECTURE

The effect of the proposed amplitude resolution improvement using PWM is verified by a behavioral simulator, namely, CppSim [7]. The main objective of the proposed architecture is to improve the amplitude resolution of a DPA. Thus, only the amplitude path is modeled in detail, whereas the phase path is modeled as ideal. The baseband input signal is the amplitude component of an EDGE signal. The resulting spectrum will be compared with the original DPA's behavioral model to show the improvement. Note that the nonideal switching waveform of a DPA is not modeled in the behavioral simulations.

In the simulation model, the input to the DPA is 10 bits, but the amplitude signal of the baseband EDGE is 15 bits. Thus, $N_{\mathrm{MSB}} + N_{\mathrm{LSB}}$ is 10, and $N_{\text{sub-LSB}}$ is 5. A 25-stage delay chain is modeled in CppSim, and the nominal delay of each stage is

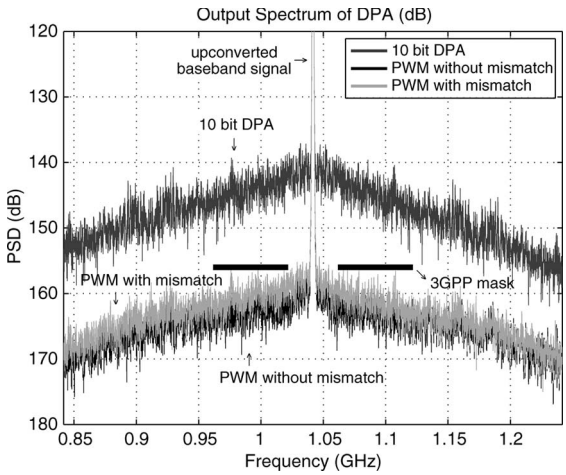

Fig. 10. Output spectrum of a 10-bit DPA and a DPA with 12-level PWM.

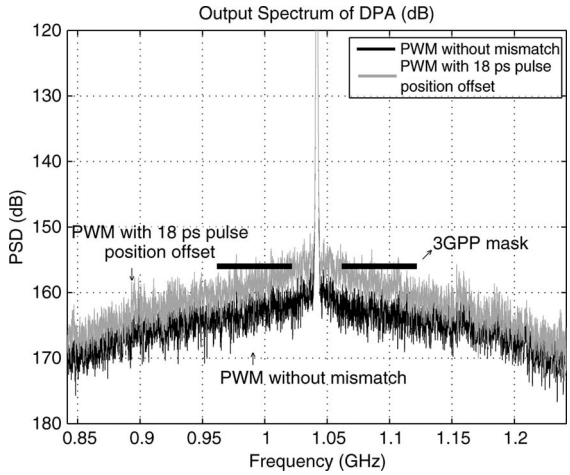

Fig. 11. PWM without position offset versus PWM with 18-ps position offset. Delay mismatch is not considered.

20 ps, which is the worst-case minimum delay of an inverter stage based on postlayout simulations in 65-nm CMOS.

To model delay mismatch of the delay chain, we first designed the PWM generator using transistor-level delay lines. A realistic delay mismatch number is then extracted using Spectre Monte Carlo simulations of the PWM generator circuits. The device Monte Carlo simulation results show about 5% of delay mismatch. However, we used 10% of delay mismatch for the behavioral simulations to be on the conservative side.

The amplitude predistortion LUT for PWM is implemented based on the simulated nominal delay of the delay elements, and its input data are 5 bits because $N_{\text{sub-LSB}}$ is 5. The carrier frequency in the simulation is 1.0417 GHz, of which the period is 960 ps. Although this is not a legal GSM/EDGE frequency, we chose it for simulation convenience since 960 ps is the integer multiple of the nominal delay of the delay stages, i.e., 20 ps.

Fig. 10 shows the spectrum of an original 10-bit DPA, a DPA with PWM, and a DPA with PWM including delay mismatch. The ETSI specifications for the RX band are also shown in the figure. The quantization noise of a DPA creates the noise skirt. The quantization noise of the system employing 12-level PWM without delay mismatch is about 18 dB lower than that of the original 10-bit DPA, which means the amplitude resolution of the DPA improves by around 2.7 bits.

Theoretically, the amplitude predistortion LUT for PWM can be built based on the exact delay of each delay stage when delay mismatch exists. However, it is impractical since a precise method of measuring the delay is required. In this brief, we assume that the LUT for PWM is implemented based on the known nominal delay of the delay elements, which means that the LUT does not take care of delay mismatch. Therefore, any delay mismatch, which is not compensated by the LUT, degrades the overall performance. Fig. 10 shows that 10% of delay mismatch raises the quantization noise by up to 3 dB, which leads to 2.2-bit resolution improvement over the original 10-bit DPA.

Fig. 11 depicts how much amplitude resolution is degraded when the position of PWM is not exactly at the center. Up to 6 dB more quantization noise is expected when the position of the PWM signal is offset by 18 ps. In a practical implementation, the Pulse Center block in Fig. 8 will properly control the pulse position. Therefore, the pulse position error should not limit the performance.

VI. Conclusion

We have proposed an architecture for amplitude resolution improvement of an RF-DAC using time as the key signal domain. The technique employs *incremental* PWM. Since it exploits the fine timing resolution of nanometer-scale CMOS technology, it does not require tighter device matching. Detailed behavioral system simulations show about 2.2-bit resolution improvement in a 1-GHz RF-DAC generating the EDGE envelope, assuming 20-ps time granularity of delay chains and including 10% of delay mismatch. The proposed architecture can simply be attached to a digitally intensive polar transmitter without major modifications. The building blocks required for the proposed architectures are a PWM generator, a fine-resolution delay controller, and an amplitude predistortion LUT for PWM.

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