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Design of Full Adder circuit using Double Gate MOSFET

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Abstract— This paper presents a design of a one bit full adder cell based on degenerate pass transistor logic (PTL) using Double Gate MOSFET. The design cell is degenerate 5-T XOR-XNOR module. This design has been compared with existing one-bit full adder cell based on degenerate pass transistor logic (PTL) designed using Single Gate MOSFET. In this paper, the proposed circuit has been analyzed for parameters like- power consumption and power delay product. The simulations of the proposed Full Adder have been performed using Tanner EDA Tool version 13.0. All the proposed design simulations are carried out at 45nm technology for various inputs like supply voltage, temperature and frequency. The decrease of 24% in power consumption has observed in proposed circuit. The results show a validity of double gate MOSFETs for designing for low power full adder circuit.

Index Terms— Full Adder; Pass Transistor Logic; Double Gate; Low Power; PDP

I. INTRODUCTION

The need of designing low power VLSI circuits has been increased immensely due to increased demand of portable devices like palmtops, cellular and mobiles. Further to integrate more number of devices on chip, scaling of device size is required. But there are number of problems in scaling of bulk MOSFETs. The problems like leakage current, drain induced barrier lowering (DIBL) effect, and other short channel affects (SCE's) degrade the performance of circuits. New device structure is needed which can work with improved performance in nanometer range of operation. A double gate MOSFET is capable device because it shows better scalability in nano circuits [1]. Double Gate MOSFET (DG MOSFET) is widely used in ultra-low power design. DG-MOSFET's has drain, source and two gates. The two gates (front and back) are electrically coupled together in double gate devices. The two gates ensure that no part of the channel is far away from a gate and it has better control over channel conductance and immunity to SCE's and reduces sub threshold leakage. DG-MOSFET can also operate in two modes such as symmetrical driven (SDDG) and independent driven (IDDG) double gate MOSFET [2-3] to design digital and analog circuits. In SDDG mode, the front and back gates are connected together and in IDDG mode, separate biasing are provided to the front and back gates. The Fig. 1(a) shows symbol of double gate MOSFET and Fig. 1(b) shows a

symmetrical and asymmetrical mode of operation of double gate MOSFETs.

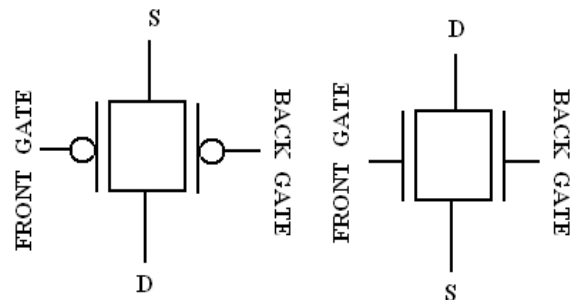


Figure 1(a). Circuit symbols for p-type and n-type DG- MOSFET transistors

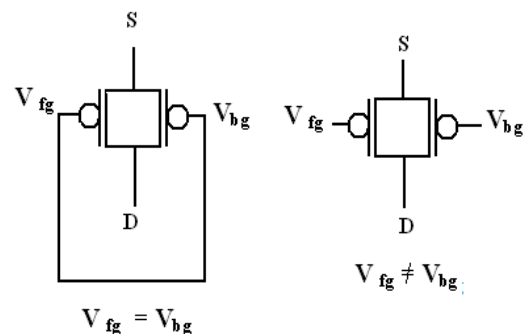


Figure 1(b). Symmetrical and independent driven double gate MOSFETs

The paper is organized into five sections. Section I give the general information for low power designing and introduce DG-MOSFET device. Section II illustrates the existing single gate based full adder cell as reported in the literature. In, section III full adder cell using DG MOSFET has been proposed. Simulations, results and comparison are given in Section IV and finally Section V concludes the paper.

II. DESIGN OF FULL ADDER USING SINGLE GATE MOSFET

The full adder is basic unit of arithmetic circuits and it is the most necessary building blocks in microprocessors, microcontrollers, ALU's and digital signal processor [4-5]. 1-bit full adder circuit has three inputs and one carry in (Cin). Various full adder circuits has been designed which emphasis

on low power, less complexity and high speed but there are several problem like degraded outputs and cannot work in ultra low power range. In this paper, high speed and low power DG- MOSFET based full adder is designed using 5-T XOR-XNOR module. Though 5T XOR-XNOR module does not satisfy all inputs, but it is sufficient to function properly in full adder applications. 5-T XOR-XNOR module [6] as given in Fig. 2(a) is designed by removing the weak pull-up transistor at the XNOR output from the 6-T design. The complementary signal will be used to generate sum and carry outputs. It is supply voltage free, so suitable for low power operations. It also avoids a latch breaking problems of XOR-XNOR module. The truth table of XOR-XNOR design is given in Fig. 2(b), in which “0⁺” and “1⁻” indicate degraded signals, i.e. $|V_{tp}|$ and $(V_{dd}-V_{tn})$, due to threshold voltage loss. In the case of both inputs equal to “0”, the XNOR output becomes floating. So this module is considered logically degenerate.

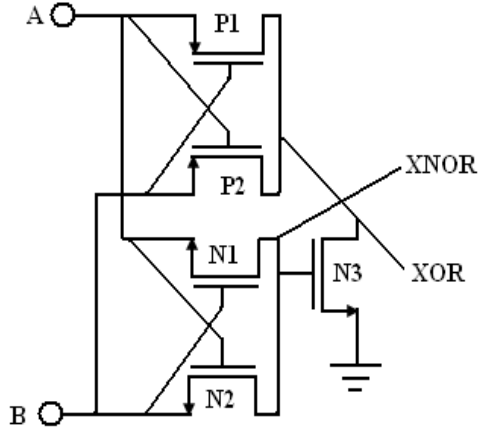


Figure 2(a). XOR-XNOR design using 5 transistors

TABLE.I TRUTH TABLE OF XOR XNOR MODULE

A	B	XOR	XNOR
0	0	0 ⁺	X
0	1	1	0
1	0	1	0
1	1	0	1 ⁻

TABLE.I illustrates a single gate MOSFET based full adder. The 5T XOR XNOR module is used to design full adder the logical equation of *Sum* and *Cout* are given as:

$$Sum = (\overline{A \oplus B})C + (A \oplus B)\overline{C} \quad (1)$$

$$Cout = (A \oplus B)C + (\overline{A \oplus B})A \quad (2)$$

The complimentary signal \overline{P} is used as control signal to realize *Sum* and *Cout* outputs with less threshold loss. The sum is observed as $Sum = P \oplus C$. Logically XOR-XNOR

modules, pass transistors P1, P2 and N1, N2 are sufficient to realize the XOR function in the *sum* module. Because the \overline{P} (XNOR input) signal could become floating, additional pass transistor P3 is added to tackle the problem. When C is equals “1” and A, B is (0, 0), C is propagated through P3, N4. When C is equal to “0” and A, B is (1, 1) the previous value of XNOR signal is retained which either “1” or “0”. This does not affect the functionality of carry module.

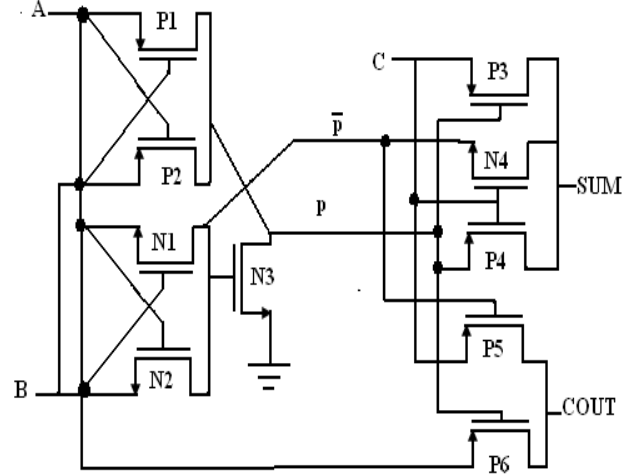


Figure 2(c). Single gate MOSFET based full adder circuit

The *carry* module uses a 2-to-1 multiplexer (P5, P6) which implements the Boolean expression:

$$Cout = P \oplus C + \overline{P} \oplus A \quad (3)$$

The multiplexer is realized by two pMOS (P5, P6). Transistor P3 is responsible for the term $\overline{P}.A$ while transistor P4 implements the term $P.C$. P3 and P4 now work in parallel to enhance the propagation of signal “0”. Although our *carry* module design has degraded signal “0⁺”, but still gives proper logical function of full adder.

III. FULL ADDER CIRCUIT USING DOUBLE GATE MOSFET

DG- MOSFET full adder circuit has been designed using the equivalent style. The full adder circuit using Double gate MOSFET has been shown in Fig. 3(a) DG- MOSFET will be constructed by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together. The two gates in DG-MOSFETs lead to increased current driving property of transistor. The DG-MOSFET structure provides electrostatic coupling for conduction channel and two gates allows additional gate length scaling by factor of 2 as compare to the single gate MOSFET [7-8]. The schematic of single gate MOSFET based full adder is implemented using double gate MOSFET in

symmetrical driven mode. There are number of adder circuits have been designed using DG-MOSFETs [9]. The proposed circuit shows better output waveforms at lower input voltages. According to the DG- MOSFET, the chip area of a p-type DG MOSFET and n-type DG MOSFET are same, and the amounts of current related to them can also be the same. The W/L ratios of transistors are taken as 1/1.

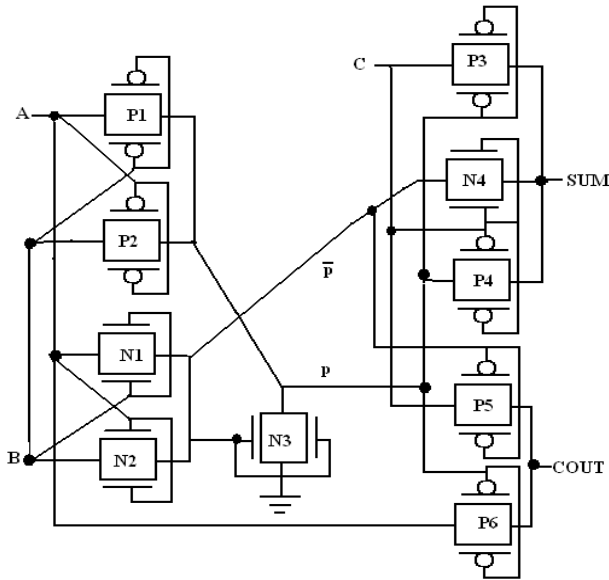


Figure 3(a). Double gate MOSFET based full adder circuit

IV. SIMULATION AND RESULTS

The simulations of proposed circuit have been done at 45 nm using level-54. The transient analysis has been performed for different input voltages, temperatures and frequency. The output waveforms of proposed circuit have been shown in Fig. 4(a).

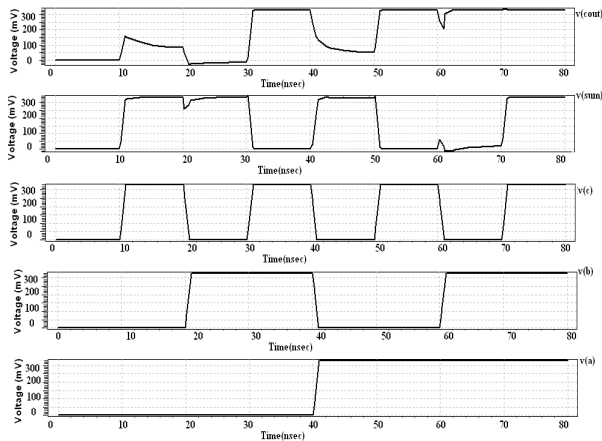


Figure 4(a). Transient analysis

A. Variation with Voltage

The variation of power consumption and power delay product with respect to input voltage respectively is observed keeping other parameters like frequency and temperature constant. The graph in Fig. 4(b) shows a power consumption comparison between single gate and double gate based full adder circuit with input voltage.

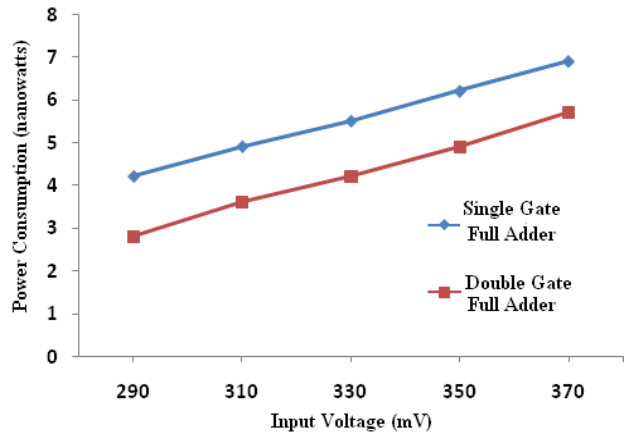


Figure 4(b). Power consumption with input voltage

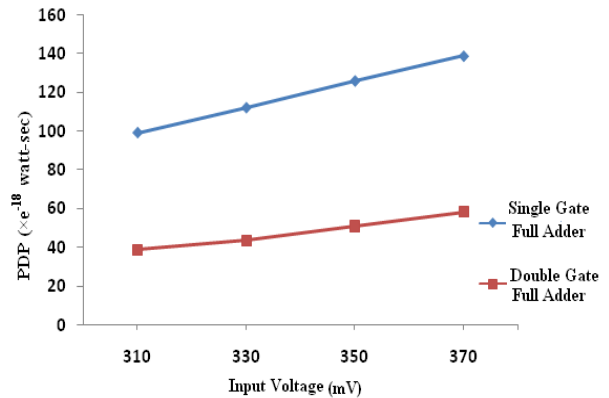


Figure 4(c). PDP with input voltage

This graph reveals 24% reduction in power consumption in DG-MOSFET based full adder. The graph in Fig. 4(c) shows comparison of power delay product with respect to input voltage and it is observed that there is 60% reduction in PDP. This shows the superiority of DG- MOSFET for ultra low power designing.

B. Variation with Temperature

The simulations are done for temperature range from 0 °C to 50 °C at 0.3V. The power consumption is increased with temperature due to phonon and scattering effects at higher temperatures. But for DG-MOSFET based full adder shows decrement of 28% in power consumption as compare to single gate MOSFET based full adder cell. The graphs depicted in

Fig. 4(d) and Fig. 4(e) illustrates a variation of power consumption as well as power-delay product with respect to temperature. PDP is increased with temperature due to increased power consumption at higher temperatures. Due to less power consumption and significant decrement in delay results into reduced power delay product for DG MOSFET design of full adder circuit. This analysis shows suitability of DG-MOSFETs for higher temperature.

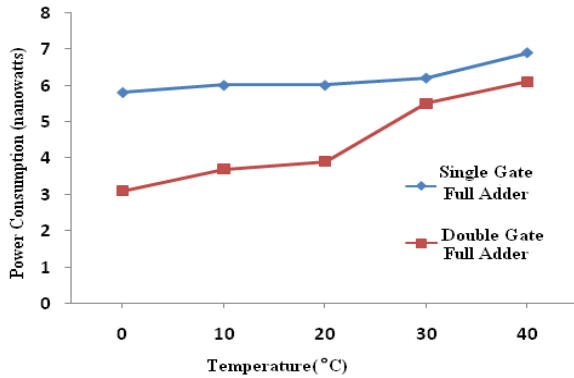


Figure 4(d). Power consumption with temperature

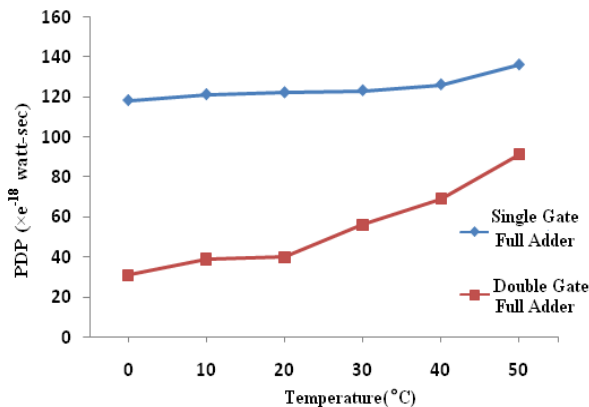


Figure 4(e). PDP with temperature

C. Variation with Frequency

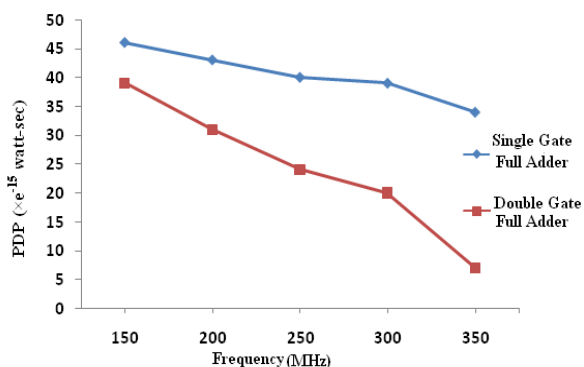


Figure 4(f). PDP with frequency

The proposed circuit is analyzed for various frequencies. As the frequency is increased, power dissipation is increased but delay has inverse relation with frequency, so it decreases. Thus overall Power delay product is decreased. The circuit is simulated for 150 MHz to 350 MHz range for 0.3 V. The graph in Fig. 4(f) shows that in double gate based full adder circuit shows decrement in PDP and it reveals a 40% decrease in PDP in case of DG-MOSFET based full adder circuit. This shows an advantage of double gate MOSFETs to design full adder circuits at higher frequencies.

V. CONCLUSION

The single gate MOSFET based full adder and DG-MOSFET based full adder circuit has analyzed for various parameters. The power consumption is reduced for DG-MOSFET based full adder cell as compare to other. It is observed that power delay product with frequency and temperature is better for DG-MOSFET based full adder circuit. The proposed circuit has higher speed and low power while it intact the digital characteristics. The proposed circuit can be used in designing low power ALU's and digital signal processors.

REFERENCES

- [1] Ravindra Singh Kushwah and Shyam Akashe, "Design and Analysis of Tunable Analog Circuit Using Double Gate MOSFET at 45nm CMOS Technology," 3rd IEEE International Advance Computing Conference (IACC), 2013.
- [2] Amara Amara, Chetan D. Parikh and D. Nagchoudhuri, "A 0.7-V Rail-to-Rail Buffer Amplifier with Double-Gate MOSFETs," Faible Tension Faible Consommation (FTFC), IEEE, 2011.
- [3] H.-S. P. Wong, "Beyond the conventional MOSFET," in Proc. 31st Eur. Solid-State Device Research Conf., 2001, p. 69.
- [4] Massimo Alioto and Gaetano Palumbo, "Analysis and Comparison on Full Adder Block in Submicron Technology" IEEE transactions on very large scale integration (VLSI) systems, vol. 10, no. 6, December 2002, pp 806-823.
- [5] Anuj Kumar Shrivastava1, Shyam Akashe2, "Design High performance and Low Power 10T Full Adder Cell Using Double Gate MOSFET at 45nm Technology", 2013 International Conference on Control, Computing, Communication and Materials (ICCCCM).
- [6] Jin-Fa Lin, Yin-Tsung Hwang and Ming-Hwa Sheu, "Low Power10-Transistor Full Adder Design Based on Degenerate Pass Transistor Logic", IEEE 2012.
- [7] Ruchika, Tripti Sharma and K. G. Sharma, "Design and Analysis of 8T Full Adder Cell Using Double Gate MOSFET", International Journal of Advances in Electronics Engineering – IJAEE, 2013.
- [8] A. K. Shrivastava and S. Akashe, "Comparative Analysis of Low Power 10T and 14T Full Adder using Double Gate MOSFET," International Journal of Computer Applications, Vol. 75(3), pp. 48-52, August 2013.
- [9] Shipra Mishra, Shelendra Singh Tomar, Shyam Akashe, "Design Low Power 10T Full Adder Using Process and Circuit Techniques" , in Proceedings of International Conference on Intelligent Systems and Control, 2013.