

The Design of Reversible BCD Digit Adders: Decreasing the Depth of Circuit

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Abstract—Reversible circuits, nowadays, have found grounds in many applications such as low power CMOS design and quantum computing. In reversible circuit design, decreasing three parameters is of interest: quantum cost, depth of the circuit and the number of garbage outputs. On the other hand, recently, decimal computer arithmetic, for the sake of its preciseness, gains popularity. Given that the BCD digit adder is the basic unit in decimal arithmetic, in this paper we propose a new reversible design for this unit with the aim of minimizing the depth of the circuit. Furthermore, we show that the proposed designing method can be applied to any other reversible circuit for reaching the minimum depth.

I. INTRODUCTION

Power dissipation is one of the important considerations in digital circuit design. A part of this energy loss is due to switches and materials. The other part arises from Landauer's principle [1] where he proved that in irreversible circuits losing one bit of information dissipates $KT \ln 2$ joules of heat energy, where K is the Boltzmann's constant and T is the absolute temperature. Although the amount of dissipating heat for room temperature is small, it can not be neglected in some applications (e.g. quantum circuit design). Furthermore, Bennett [2] showed that reversible circuits do not lose information due to the one-to-one mapping between inputs and outputs; hence no extra energy loss.

In the design of reversible circuits two restrictions should be considered:

- Fan-out is not permitted
- Loops are not permitted

Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa [3].

From the point of view of reversible circuit design there are three parameters for determining the complexity and performance of circuits [4]:

- **Quantum cost (QC):** the number of 1×1 or 2×2 reversible gates which are used in circuit.
- **The number of garbage outputs (GO):** The number of dummy (unused) outputs which are added in order to make the circuit reversible.

- **Depth:** The number of 1×1 or 2×2 reversible gates which are in the longest path from input to output.

Reduction of these three parameters simultaneously is difficult. Therefore, one or two of them are usually opted as the main parameter for minimization and try to reduce others as much as possible. In this paper a new method for designing reversible circuits, with the aim of minimizing the depth of the circuit is proposed and applied to the reversible one digit BCD adder. Since depth in reversible circuits can be considered as the latency in classic circuits, the proposed adder is based on Carry-Look-Ahead (CLA) topology which has been proved to be the fastest [5].

The rest of paper is organized as follows: reversible gates are explained in section 2; the prerequisites of BCD adders are discussed in section 3 while in section 4 the proposed design is presented; section 5 compares the new design with previous works and finally section 6 summarizes the outcome of this paper.

II. REVERSIBLE GATES

An $n \times n$ reversible circuit consists of n inputs and n outputs with mapping of each input assignment to a unique output assignment and vice versa. There are two main types of reversible gates: Toffoli [6] and Fredkin [7]. An n -bit Toffoli gate passes the first $(n-1)$ inputs to output unaltered (as control signals) and for the last output the n th input inverts (as target signal) if all previous $(n-1)$ signals are '1'.

Some types of reversible gates are as follows:

1×1 not Gate: it is clear that one-input-one-output inverter gate is reversible.

2×2 Feynman Gate: The first input (a) controls the second one (b) such as shown in Fig. 1. This gate is also known as CNOT gate [8].

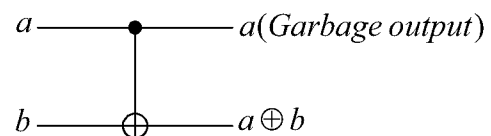


Fig. 1. 2×2 Feynman gate

Since fan-out is not permitted in reversible circuits, a 2×2 Feynman gate can be used instead (see Fig. 2).

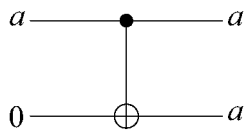


Fig. 2. Fan-out gate

3×3 Toffoli Gate: This gate passes the first two inputs to output unaltered (as control signals) and inverts the last input (as target signal) if two previous inputs are '1'. Fig. 3 depicts a 3×3 Toffoli gate [6].

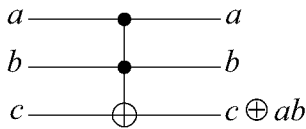


Fig. 3. 3×3 Toffoli gate

3×3 Fredkin Gate: this gate passes the first input unaltered; second and third inputs are swapped, if the first input is '1'. A 3×3 Fredkin gate is depicted in Fig. 4 [7].

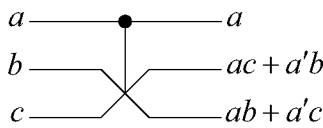


Fig. 4. 3×3 Fredkin gate

Since the implementation of OR, AND, NOT and Fan-Out gates is possible through the use of Fredkin gate, this gate is proved to be universal. Fig. 5 shows this possibility [9].

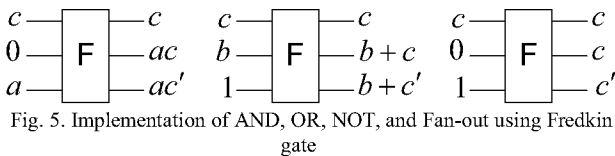


Fig. 5. Implementation of AND, OR, NOT, and Fan-out using Fredkin gate

3×3 New Gate: this gate is depicted in Fig. 6. Equations between inputs and outputs are also shown in figure [9].

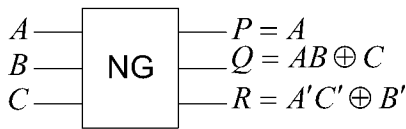


Fig. 6. New Gate

3×3 New Toffoli Gate: the block diagram and input-output equation of this gate is shown in Fig. 7 [9].

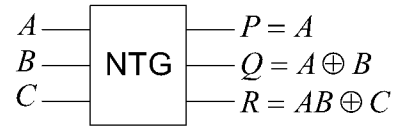


Fig. 7. New Toffoli Gate

III. THE ONE DIGIT BCD ADDERS

A one digit BCD adder is a special type of adder that adds two BCD digits and converts the result into its equivalent BCD number. Adding two BCD digits can be partitioned into 3 steps:

- 1) Binary addition
- 2) Over-9 detection
- 3) Correction

In the first step a simple 4-bit binary addition is performed on two input digits (each digit has 4-bits) and 1-bit input carry. In the second part an over-9-detector detects if the result of the first step is more than 9 or not. And finally in the third step if the output of detector is 1, then the sum is added by 6 [10].

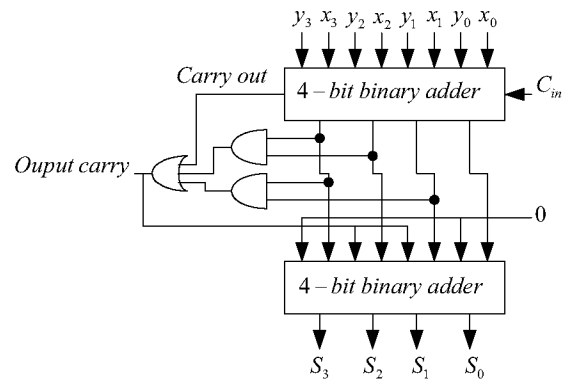


Fig. 8. BCD digit adder circuit

IV. REVERSIBLE IMPLEMENTATION OF THE BCD DIGIT ADDER

In this section we first introduce NAND gate as the basic element in this design; then explain how to design a BCD digit adder using CLA and finally the proposed circuit is presented.

A. Reversible NAND gate

Every logic function can be implemented using NAND gate. If we add the Fan-out gate to our inventory, then this is also true in reversible logic. To achieve this goal, we should first design the reversible NAND gate. A $(k+1)$ -CNOT gate which its last input is 1, can be considered as a k -input NAND gate (see Fig. 9). The same approach can be applied to design a reversible AND gate by letting the last input be '0' [11].

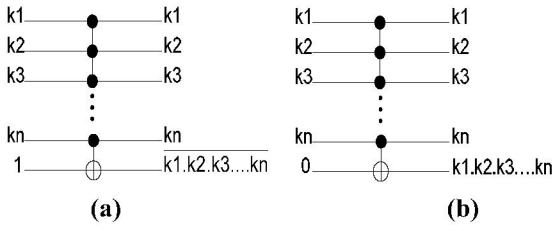


Fig. 9. Reversible implementation of (a) NAND (b) AND gate using k -CNOT

The defect of this method is increasing the quantum cost, depth, and number of garbage outputs for the design of NAND gates. Because of this, we propose another technique. Algorithm 1 describes this method.

Algorithm 1 (Designing Reversible NAND gates):

- I. Convert k -input NAND gates ($k > 2$) into 2-input AND/NAND gates.
- II. Replace each 2-input AND (NAND) gate with the reversible NTG while its last input is 0 (1). ■

The Step I of the above algorithm can be done through the use of a binary tree. The whole topology is a binary tree where the nodes are 2-input AND gates, the root is a 2-input NAND gate, and the inputs are the leaves of this tree. The NTG used in step 2, was described in Section 2. By letting 1 (0) as its last input, then the last output is the NAND (AND) operation of other two inputs of NTG.

The QC and depth of NTG gate is 4 [9]. Table I illustrates the cost and depth of NAND gates having different number of inputs using this method.

Table I
Quantum Cost and Depth of NAND gates

# of Inputs	2	3	4	5	n
QC	4	8	$\frac{1}{2}$	$\frac{1}{6}$	$4 \times (n-1)$
Depth	4	8	8	$\frac{1}{2}$	$4 \times \lceil \log n \rceil$

B. Implementation of the BCD digit adder based on Carry-Look-Ahead technique

In 1971 Schmoockler and Weinberger proposed a design for implementing BCD digit adder using CLA approach [10]. Consider two 4-bits operands A and B which are to be added as follows:

$$\begin{array}{r}
 A_8 \quad A_4 \quad A_2 \quad A_1 \quad C_{in} \\
 + \quad B_8 \quad B_4 \quad B_2 \quad B_1 \\
 \hline
 C_{out} \quad S_8 \quad S_4 \quad S_2 \quad S_1
 \end{array}$$

If this were a 4-bit binary addition, one could obtain the carry into each bit position from the lower order position to the right, and obtain the sum directly from

$$S_i = (A_i \oplus B_i) \oplus C_{i-1}$$

For the input variables in weights 2, 4 and 8 of each digit, two new functions, called K and L were defined. If sum of these columns is 10 or greater then K is true. L function is true when this sum is 8 or greater. Thus, If C_1 is the carry from column 1, the digit carry is

$$C_{out} = K + LC_1$$

It is apparent that K represents a carry generate function and L represents a carry propagate function. For obtaining the Boolean functions of K and L , three other functions were defined [10]:

$$P_i = A_i + B_i, \quad G_i = A_i B_i$$

$$H_i = A_i \oplus B_i = A_i \bar{B}_i + \bar{A}_i B_i$$

According to the definition of K and L , we have

$$K = \{sum \geq 10\} = G_8 + P_8 P_4 + P_8 P_2 + G_4 P_2$$

$$L = \{sum \geq 8\} = P_8 + G_4 + P_4 G_2$$

Now according to the auxiliary functions defined above, Boolean expression for each S_i is obtained as follows [10]:

S_1 is obtained in the usual manner of a binary sum:

$$S_1 = (A_1 \oplus B_1) \oplus C_{in} = H_1 \oplus C_{in}$$

According to the correction step in BCD digit adder, S_2 is dependent on C_{out} .

$$S_2 = H_2 \oplus C_1 \oplus C_{out}$$

Expression for S_4 and S_8 will be obtained as follows:

$$\begin{aligned}
 S_4 = & \bar{P}_4 G_2 + \bar{P}_8 H_4 \bar{P}_2 + (\bar{P}_8 \bar{P}_4 P_2 + G_4 G_2 + \\
 & P_8 P_4) C_1 + (G_8 + H_4 H_2) \bar{C}_1
 \end{aligned}$$

$$S_8 = (G_8 + H_4 H_2) \bar{H}_8 C_1 + L \bar{C}_{out}$$

C. The proposed reversible BCD digit adder

As mentioned before the purpose of this paper is the design of BCD digit adder with the aim of minimizing its depth. To achieve this, we use the carry-look-ahead adder (CLA) topology. The required Boolean expressions were mentioned in previous subsection; but here to achieve better result, we use the extended form of some of these expressions.

$$L = A_8 + B_8 + A_4 B_4 + A_4 A_2 B_2 + B_4 A_2 B_2$$

$$C_{out} = A_8 A_1 B_1 + B_8 A_1 B_1 + A_4 B_4 A_1 B_1 + A_4 A_2 B_2 A_1 B_1 \\ + B_4 A_2 B_2 A_1 B_1 + A_8 B_8 + A_8 A_4 + A_8 B_4 + B_8 A_4 + \\ B_8 B_4 + A_8 A_2 + A_8 B_2 + B_8 A_2 + B_8 B_2 + A_4 B_4 A_2 + \\ A_4 B_4 B_2$$

$$S_4 = \bar{A}_4 \bar{B}_4 A_2 B_2 + \bar{A}_8 \bar{B}_8 H_4 \bar{A}_2 \bar{B}_2 + \bar{A}_8 \bar{B}_8 \bar{A}_4 \bar{B}_4 A_1 B_1 A_2 + \\ \bar{A}_8 \bar{B}_8 \bar{A}_4 \bar{B}_4 A_1 B_1 B_2 + A_4 B_4 A_2 B_2 A_1 B_1 + A_8 A_4 A_1 B_1 + \\ A_8 B_4 A_1 B_1 + B_8 A_4 A_1 B_1 + B_8 B_4 A_1 B_1 + A_8 B_8 \bar{A}_1 + \\ A_8 B_8 \bar{B}_1 + H_4 H_2 \bar{A}_1 + H_4 H_2 \bar{B}_1$$

$$S_8 = A_8 B_8 A_1 B_1 + H_4 H_2 \bar{H}_8 A_1 B_1 + L \bar{C}_{out}$$

By and large, the proposed method for designing the reversible circuit with the minimum depth is described in Algorithm 2, below.

Algorithm 2 (Design of a reversible circuit with the minimum depth):

- I. Design the Boolean expressions with classic NAND gates in two levels.
- II. Implement each k -input NAND gate using 2-input AND/NAND gates.
- III. Substitute each 2-input AND/NAND gates with its reversible equivalent NTG.
- IV. Add Fan-out gates wherever is needed in the circuit. ■

It is trivial that for reversible NAND gates with odd number of inputs the depth of the path from the last input to the output is less than other inputs. Hence, putting this path into the total critical path of the circuit leads to the minimum depth. Fig. 10 shows an example for a 5-input NAND gate.

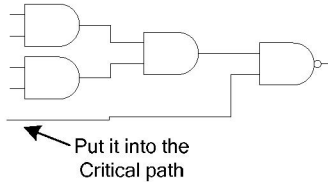


Fig. 10. The example for a 5-input NAND gate

By using this algorithm the depth of each function of the reversible BCD digit adder is obtained as shown in Table II.

Table II
The depth of BCD digit adder functions

Function	S1	S2	S4	S8	C_{out}
Depth	7	34	33	41	34

According to Table II the depth of the proposed BCD digit adder equals that of S_4 which is 41.

V. COMPARISON WITH PREVIOUS WORKS

In the recent years various designs were presented for reversible BCD adder. Here we describe some of them concisely.

In 2005 and 2006, Babu et. al. [12] and [9] proposed a reversible BCD adder which was the first design in this field. In these designs BCD adder is composed of two reversible 4-bit adders, a combinational detector circuit and some fan out gates. 4-bit adders are made of four reversible FA. The above authors tried to use the least number of gates and garbage outputs.

In 2007 Mohamadi et. al. [13] presented a design which is minimized for the quantum cost.

In the late 2007 Thomsen et al. [14] proposed an optimized reversible BCD adder where the “the number of transistors” instead of the quantum cost was measured and minimized.

Finally, in 2008 Biswas et al. [15] proposed another reversible BCD adder. They took advantage of the carry skip topology and reached faster design for n -digit BCD adders. However, their 1-digit BCD adder doesn't show any improvement with respect to the previous methods.

Table III illustrates a comparison between previous designs and ours. The depth of the proposed circuit is the least in comparison with the previous works known to us, at the expense of more quantum cost and garbage outputs.

Table III
Comparison of reversible BCD digit adders

	Ours	[12]	[9]	[13]	[14]	[15]
Depth	41	83	67	67	109	75

VI. CONCLUSIONS

In this paper a new method for designing reversible circuits, with the aim of reducing the depth of the circuit, was proposed. The method is based on the design of reversible AND/NAND gates by means of New Toffoli Gate (NTG). We took advantage of the latter method to design a reversible BCD digit adder. We used the carry-look-ahead adder (CLA) topology, which is believed to be the fastest design, for the proposed BCD digit adder. The comparison of the proposed adder with those of the previous works showed that the depth of the new design is about 38% less than that of the best previous work, at the expense of more quantum cost and garbage outputs which were not the goal of minimization.

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