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An Efficient Reversible Design of BCD Adder

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Abstract—**Nowadays, Reversible logic plays an important role in vlsi design. It has voluminous applications in quantum computing, optical computing, quantum dot cellular automata and digital signal processing. Adders are key components in many computational units, so design efficient binary coded decimal (BCD) adder using reversible gates is needed. It is not possible to calculate quantum cost without implementation of reversible logic. This paper propose a new design for BCD adder that optimized in terms of quantum cost, memory usage and number of reversible gates. The important reversible gates used for reversible logic synthesis are NOT gate, CNOT gate, Toffoli gate, peres gate, TR gate and MTSG gate.**

***Key words*—Reversible logic, quantum cost, mtsg gate**

I. INTRODUCTION

Power dissipation is one of the most important factors in VLSI circuit design. Irreversible logic circuits dissipate KT*Log2 joules heat energy[1]. Where K is Boltzmann's constant and T is the absolute temperature at which the computation is performed. The amount of energy dissipate in a system bears a direct relationship to the number of bits erased during the computation. Some bits erased means some information is lost. Bennet showed that the KT*Log2 joules energy dissipation would not occur if a computation is carried out in a reversible manor. Reversible computation can be performed through circuits that do not lose information[11].

As the Moore's law continues to hold, the processing power doubles every 18 months[1]. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase the information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. The main challenges of designing reversible circuits are to reduce number of gates, memory usage, delay and quantum cost. This paper presents a new design of reversible BCD adder. The hardware complexity of this design is very less when compared to the existing once.

II. BASIC DEFINITIONS OF REVERSIBLE LOGIC

In this section, the basic definitions and ideas to the reversible logic and few reversible gates which are used and relevant with this research work.

A. Reversible logic

It is an n-input, n-output logic function in which there is a one-to-one correspondence between the inputs and outputs[12]. Because of this one to one mapping the input vector can be uniquely determined from the output vector.

B . Quantum cost

Quantum cost refers of to the cost of circuit in terms of the cost of primitive gate. It is calculated knowing the number of primitive reversible logic gates required to realize the circuit[10].

C. Delay

The delay of a logic circuit is the maximum number of gates in a path from any input line to any output line. This definition is based on the following assumptions[11]:

(i) Each gate performs computation in one unit time.
(ii) All inputs to the circuit are available before the Computation begins.

E . Hardware complexity

Hardware complexity refers to the total number of logic operations in a circuit. Means the total number of AND, OR and EXOR operation in a circuit.

F . Ancilla inputs

This refers to the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function[7].

G . Garbage outputs

Garbage outputs are the unutilized outputs in reversible circuits which maintain reversibility but do not perform any useful operations[3].

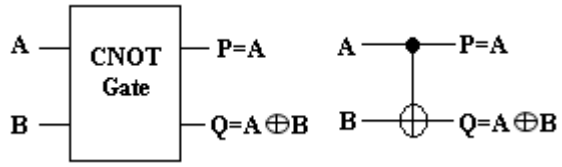
III. REVERSIBLE LOGIC GATES

A . CNOT GATE

Cnot gate is also known as controlled-not gate. It is a 2*2 reversible gate. The Cnot gate can be described as:

Iv = (A, B)
Ov = (P= A, Q= A ⊕B)

Iv and Ov are input and output vectors respectively. Quantum cost of Cnot gate is 1[14]. Figure 1 shows a 2*2 Cnot gate and its symbol.



(a) Block diagram (b) symbol

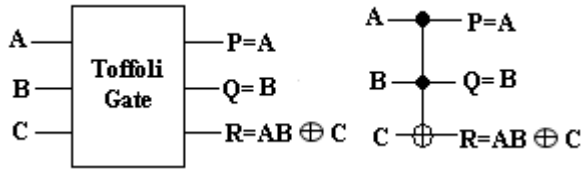
Figure 1: CNOT Gate

B . TOFFOLI GATE

Toffoli gate is a 3*3 reversible gate[14]. The input vector is I(A,B,C) and output vector is O(P,Q,R). the Toffoli gate can be described as:

Iv = (A, B, C)
Ov= (P=A, Q=B, R = AB⊕C)

Quantum cost of Toffoli gate is 5. Figure 2 shows a 3*3 Toffoli gate and symbol.



(a) Block diagram (b) symbol

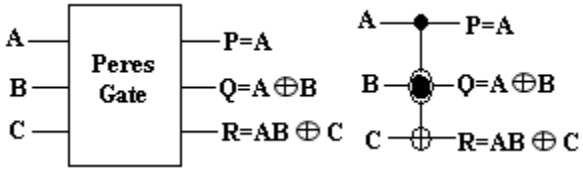
Figure 2: Toffoli Gate

C. PERES GATE

Peres gate is a 3*3 reversible gate. It is also known as New Toffoli gate. It is constricted from CNOT gate and Toffoli gate[11]. The Peres gate can be described as:

I_v = (A, B, C)
O_v = (P = A, Q = A⊕B, R = AB⊕C)

I_v and O_v are input and output vectors orderly. Quantum cost of Peres gate is 4.
The Peres gate and its symbol is shown in figure 3.



(a) Block diagram (b) symbol

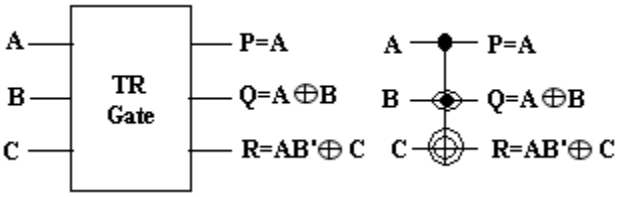
Figure 3: Peres Gate

D. TR GATE

TR gate full name is Thapliyal-Ranganathan gate. It is a 3*3 reversible gate[14]. The TR gate can be described as:

I_v = (A, B, C)
O_v = (P = A, Q = A⊕B, R = AB'⊕C)

I_v and O_v are input and output vectors orderly. Quantum cost of TR gate is 4. The TR gate and its symbol is shown in figure 4.



(a) Block diagram (b) symbol

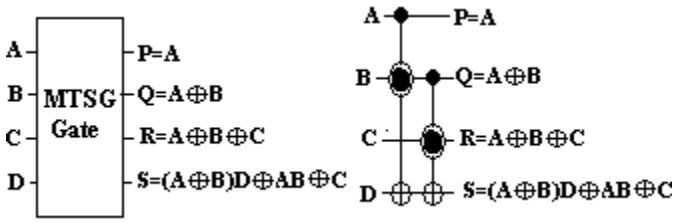
Figure 4: TR Gate

E. MTSG GATE

MTSG gate is a 4*4 reversible gate. The MTSG gate can be described as:

I_v = (A, B, C, D)
O_v = (P = A, Q = A⊕B, R = A⊕B⊕C,
S = (A⊕B)C⊕AB⊕D)

I_v and O_v are input and output vectors orderly. Quantum cost of MTSG gate is 6[11]. MTSG will be very useful to design reversible circuits as the quantum cost of the MTSG is very low as compared to the TSG gate[11]. it is constricted from cascading of two Pares gates. By providing '0' in the D input, easily realize the full-adder from the MTSG gate. A reversible full adder can be realized at least one gate. For designing n-bit binary ripple carry adder n MTSG gates are required. The MTSG gate and its symbol is shown in figure 5.



(a) Block diagram (b) symbol

Figure 5: MTSG Gate

IV. BLOCK DIAGRAM OF BCD ADDER

A BCD adder is a circuit that adds two BCD numbers and produces a sum also in BCD form. Figure 6 shows the block diagram of BCD adder. A BCD adder must include three major parts[15]. Those are

(i) Binary adder
(ii) Over 9 detection unit
(iii) Correction unit

Binary adder performs addition operation on two BCD numbers and one-bit carry input.
Over 9 detection unit recognizes if the result of first part is more 9or not[16]. If the result is more than 9 it produces 1 otherwise 0.

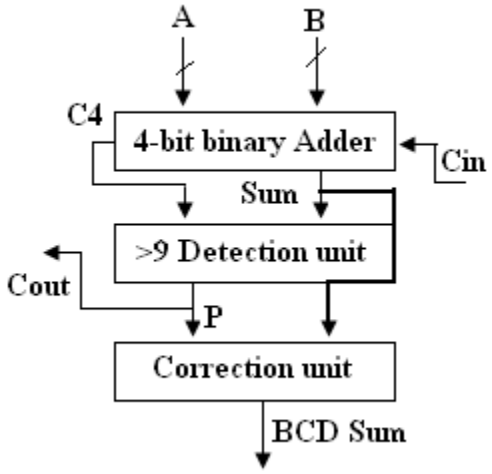


Figure 6: Block diagram of BCD adder

Correction unit, if the output of detector is 1then the sum is added by 6, else added by 0.

A conventional BCD adder is shown in figure 7. The first part 4-bit binary adder is cascade of four full adders. The second part detection unit is constructed by using two AND gates and one OR gate[16]. The third part correction unit adds 0 to the binary number if the binary result is less than 10 and adds 6 to the binary result if it is more than 9[15]. Binary full adder is a basic circuit for designing binary arithmetic units such as n-bit binary adder, sub tractor and multiplier. In same manor a BCD adder/subtract or is a basic circuit for designing BCD arithmetic units such as BCD n-bit adder/sub tractor.

V. EFFICIENT DESIGN OF REVERSIBLE BCD ADDER

This is the equivalent design of the approach shown in figure 7. Proposed reversible BCD adder optimized for the number of reversible gates, memory usage and quantum cost. The proposed design of BCD adder is shown in figure 8. In first part 4 MTSG gates are connected in series. It can

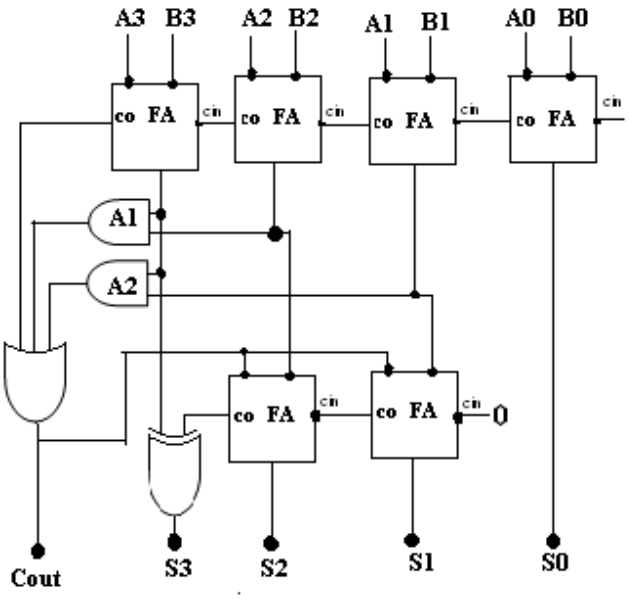


Figure 7: An irreversible BCD adder

work as 4-bit binary adder produce sum and carry[11]. Second part is equivalent design of over 9 detection unit and correction unit[14].

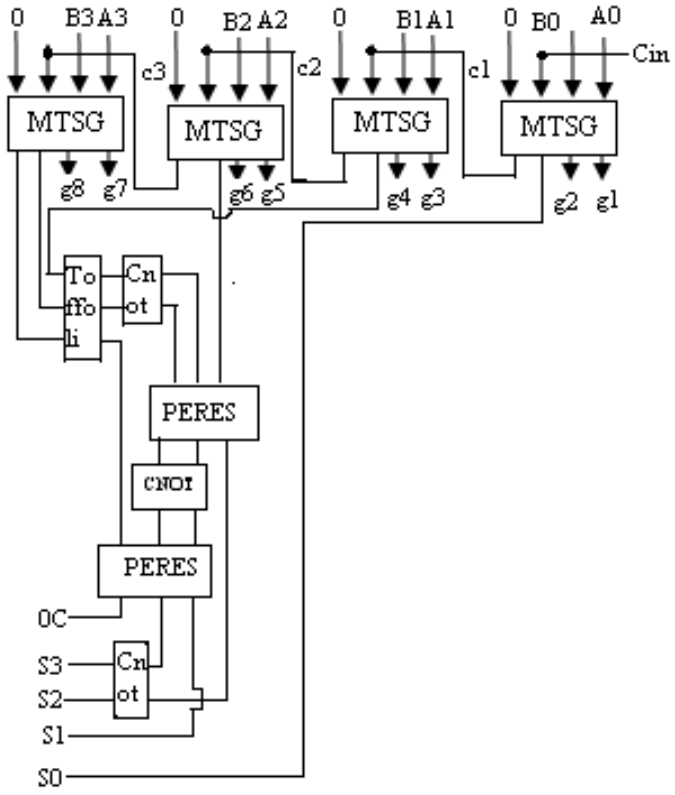


Figure 8: Proposed design of reversible BCD adder

A . Quantum cost calculation

For n-bit proposed methodology needs n MTSG gates working in series thus in this stage has the quantum cost is 6n. In next stage (n-3) toffoli gates are working in series thus in this stage quantum cost is 5(n-3). In next stage (n-3) CNOT gates are working in series thus in this stage quantum cost is (n-3). In next stage (n-3) Peres gates are working in series thus in this stage quantum cost is 4(n-3). In next stage (n-3) CNOT gates are working in series thus in this stage quantum cost is (n-3). In next stage (n-3) Peres gates are working in series thus in this stage quantum cost is 4(n-3). In next stage (n-3) CNOT gates are working in series thus in this stage quantum cost is (n-3).

Thus the total quantum cost of n bit reversible BCD adder is 6n+5(n-3)+n-3+4(n-3)+n-3+4(n-3)+n-3=22n-48. In this paper we are discuss about 4-bit reversible BCD adder so quantum cost of proposed reversible BCD adder is 40. Number of reversible gates used in this design is 10.

VI. RESULTS AND DISCUSSION

The proposed reversible BCD adder design has quantum cost 4 and delay is 11.228ns. To construct proposed BCD adder 10 reversible gates and 10 BELS and 6 slices are required. A comparison with the existing designs of the Reversible BCD adder is illustrated in Table I. the design in [14] is the best existing design literature considering the Number of reversible gates, Quantum cost, Delay and BELS. It Needs 36 reversible gates and has the quantum cost 70 and it require 9 slices. The delay of design in [14] is 11.153ns. it can be observed from the comparison table that the proposed design is better than the design in [14] in terms of number of reversible gates, area, delay, quantum cost. Thus the proposed design is efficient compared to existing designs.

TABLE I

A COMPARISION OF REVERSIBLE BCD ADDERS

BCD Adder	No.of slices	No.of gates	Quantm cost	Delay (ns)	BELS
Existing [14]	**9**	**36**	**70**	**12.15**	**22**
Proposd Design	**6**	**10**	**40**	**11.22**	**10**

VII. Conclusion

In this paper, reversible logic was implemented for BCD adder. By comparing the existing design with proposed design is less costly in terms of number of gates and quantum cost and delay and area and BELS. The proposed design is highly optimized. The efficient design of the BCD adder depends on the Design methodology used for designing the reversible ripple carry adder and the reversible binary to BCD converter. Thus for future research, efficient design schemes for reversible ripple carry adder and the reversible binary to BCD converter is an interesting area to investigate.

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