Optimized design of BCD adder and Carry skip BCD adder using reversible logic gates

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Abstract: Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nano technology and other low power digital circuits. In the present paper an optimized and low quantum cost one digit BCD adder and an optimized one digit carry skip BCD adder using new reversible logic gates are proposed. The proposed work is best compared to the other existing circuits.

Keywords— Reversible logic circuits, reversible BCD adder, carry skip BCD adder, quantum computing.

I. INTRODUCTION

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, DNA computing, quantum computing and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2].

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. Reversible circuits are constructed using reversible logic gates. These reversible circuits not only produce unique output vector from each input vector but also the input can be reconstructed from the outputs. A reversible circuit should be designed using a minimum number of reversible gates. Fan-out and loops are not allowed in reversible logic circuits [3]. However fan-out and feedback can be achieved by using additional gates.

The complexity and performance of the circuit is decided on the following parameters [4, 5, and 7].

(i) **Garbage outputs:** The number of unused outputs present in the reversible logic circuit.
(ii) **Number of reversible gates:** Total number of reversible gates used in the circuit.
(iii) **Delay:** Maximum number of unit delay gates in the path of propagation of inputs to outputs. It represents the total number of reversible gates used between the primary inputs and the outputs of a reversible logic circuit.
(iv) **Constant inputs:** The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function.
(v) **Quantum cost:** The number of 1x1 or 2 x 2 reversible logic gates used in the quantum equivalent of the reversible circuit.

The synthesis of a reversible logic circuit should have following optimization parameters [4-18]:

- minimum number of gates
- minimum number of garbage outputs
- minimum number of constant inputs
- minimum delay

Decimal addition plays an important role in various microprocessors and other future computing circuits. Therefore circuits designed to perform decimal addition using binary methods must be fast and must incorporate the required correction to produce accurate decimal sum. The present paper proposes an optimized design of a BCD adder and a carry skip BCD adder using new reversible logic gates. The proposed 1 digit BCD adder is constructed using a minimum number of reversible logic gates and it produces the least number of garbage outputs compared to other exisiting circuits and therefore it can used to build more complex arithmetic circuits using reversible logic gates.

This paper is organized as follows: Section II gives the brief introduction to some of the important basic reversible logic gates. In Section III the new gates used in the proposed design of BCD and carry skip BCD adder circuits are explained. In Section IV, the conventional 1 digit BCD adder and 1 digit carry skip BCD adder circuit and its implementation using new reversible gates are described. Section V gives the reversible logic implementation of the proposed designs of these adders. Section VI gives the results and discussion and also the comparison of proposed design with other existing circuits. Finally Section VII concludes with a scope for further research.

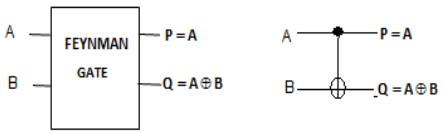
II. REVERSIBLE LOGIC GATES

At present there are many 3x3 reversible logic gates such as Fredkin gate, Toffoli gate, Double Feynman gate, Peres gate [3-8]. The quantum cost of each reversible logic gate is an important optimization parameter [7]. The quantum cost of a 1x1 reversible gate is assumed to be zero. The quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V^+ and CNOT gates present in their quantum circuit. V is the square root of NOT gate and V^+ is its hermitian. The V and V^+ quantum gates have the following properties:

$$V * V = NOT \quad (1)$$
$$V * V^+ = V^+ * V = 1 \quad (2)$$
$$V^+ * V^+ = NOT \quad (3)$$

Important reversible logic gates are,

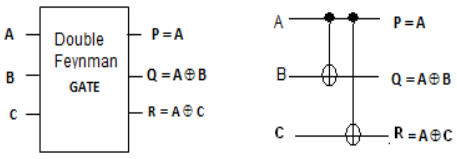
Feynman gate: Fig.1 shows a 2 x2 Feynman gate [3]. The input vector is I (A, B) and the output vector is O (P, Q) and the relation between input and output is given by P=A, Q = A⊕ B. Since it is a 2 x 2 gate, it has a quantum cost of 1 [8]. It is used to copy the input without producing garbage bits.



(a) Feynman gate (b) Quantum implementation of Feynman gate

Fig .1 Feynman gate and its quantum implementation

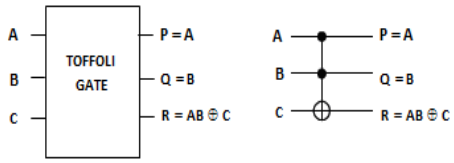
Double Feynman gate (F2G): Fig. 2 shows a 3 x 3 Double Feynman gate [4]. The input vector is I (A,B,C) and the output vector is O(P,Q,R) and output is defined by P = A , Q = A⊕B , R = A⊕C. Quantum cost of Double Feynman gate is 2.



(a) Double Feynman gate (b) Quantum implementation of Double Feynman gate

Fig. 2 Double Feynman gate and its quantum implementation

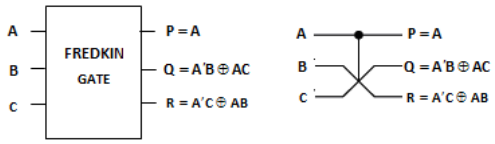
Toffoli gate (TG): Fig. 3 shows a 3 x 3 Toffoli gate [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by P = A, Q = B, R = AB⊕C.



(a) Toffoli gate (b) Quantum implementation of Toffoli gate

Fig.3 Toffoli gate and its quantum implementation

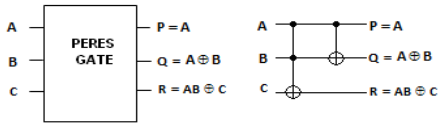
Fredkin Gate (FG): Fig 4 shows a 3 x 3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.



(a) Fredkin gate (b) Quantum implementation of Fredkin gate

Fig.4 Fredkin gate and its quantum implementation

Peres Gate (PG): Fig 5 shows a 3x3 Peres gate [6]. The input vector is I (A, B, C) and the output vector is O (P,Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

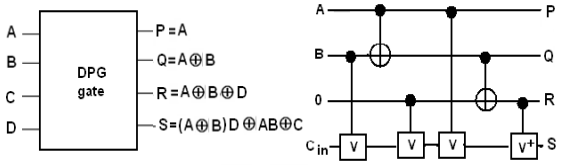


(a) Peres gate (b) Quantum implementation of Peres gate

Fig.5 Peres gate and its quantum implementation

III. PROPOSED REVERSIBLE GATES

Double Peres gate (DPG): Fig 6 shows a Double Peres Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). P = A, Q = A⊕B, R = A⊕B⊕D and S= (A⊕B) D ⊕AB⊕C. The full adder using DPG is obtained with C=0 and D= C_{in} and its quantum cost is equal to 6 from [9] and is similar to PFAG [11, 12, 21].



(a) Double Peres gate (b) Quantum implementation of Double Peres gate as a full adder

Fig.6 Double Peres gate and its quantum implementation

SCLgate (SCLG): Fig.7 shows a 4 x 4 SCL gate [12]. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S) and the relation between input and output is given by,

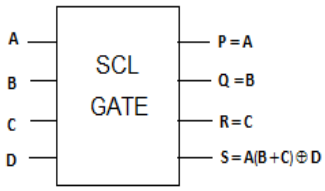


Fig.7 Six-correction logic gates

There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum [12].In the present paper SCL gate (Six Correction Logic) is used for the required correction in the BCD addition.

In a BCD adder, the correction logic which generates the C_{out} is given by,

$$C_{out} = S_3S_2 + S_3S_1 + C_4 \quad (4)$$

The above equation can also be expressed without changing its functionality into,

$$C_{out} = C_4 \oplus S_3 (S_2 + S_1) \quad (5)$$

The proposed SCL gate gives the required correction logic at the output $S=C_{out}$ and also passes the inputs A= S3, B=S2 and C=S1 to P, Q and R respectively as shown in fig.8,thereby avoiding the fan-out problem present in the BCD adder and carry skip adder circuit given in the paper [14-17].

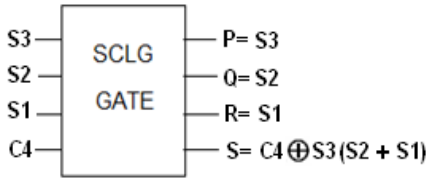


Fig.8 SCL gate producing Cout

IV CONVENTIONAL BCD ADDER AND CARRY SKIP BCD ADDER

a) Conventional BCD adder

Fig 9 and Fig.10 shows the conventional one digit BCD adder and one digit Carry skip BCD adder circuits.

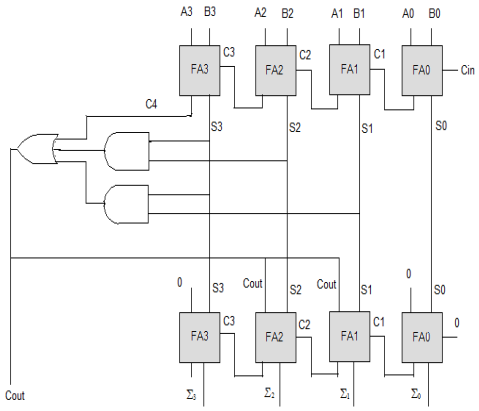


Fig.9 One digit BCD adder

The correction logic circuit adds 6 to the sum obtained from the first adder to generate the correct BCD sum following the rules of BCD addition.

b) Conventional Carry skip adder

The circuit is as shown in fig 10. It uses two four bit adders, carry skip logic circuit and a correction logic circuit. The carry skip BCD adder is faster than the above BCD adder as it skips the propagation of carry input if Z=1. The carry propagate input $Z = Z_0.Z_1.Z_2.Z_3$ is generated at the output of a 4-input AND gate where $Z_0 = (A_0 \oplus B_0)$, $Z_1 = (A_1 \oplus B_1)$, $Z_2 = (A_2 \oplus B_2)$ and $Z_3 = (A_3 \oplus B_3)$. When Z=1, the carry input C_{in} is propagated to reach C_{out} , otherwise it is skipped without propagating through the full adders. If Z=0, C_4 is propagated to C_{out}. Also whenever C_{out} = 1, correction logic adds 6 to the sum to generate the correct BCD sum as per rules of BCD addition.

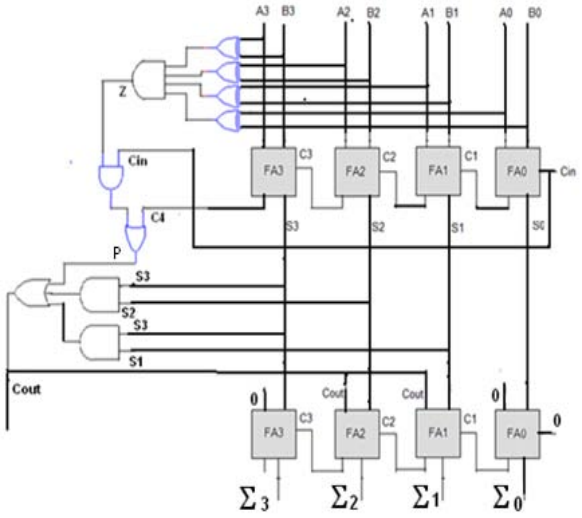


Fig.10 One digit Carry skip BCD adder

IV REVERSIBLE LOGIC IMPLEMENTATION OF ADDERS

a) **One digit BCD adder using reversible logic gates:**

The BCD adder can be constructed using reversible gates. The proposed BCD adder uses Double Peres gates for the construction of 4-bit parallel adder to add two BCD inputs. The total number of garbage outputs generated from the reversible parallel adder is equal to eight as shown in fig.11.

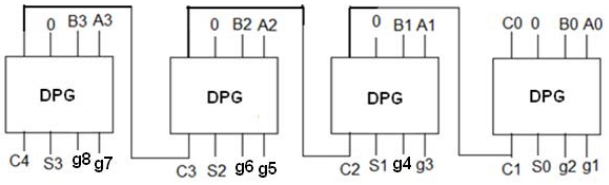


Fig.11 4 bit parallel adder using DPG gates

The overflow detection uses one SCL gate. The second adder which should add six (0110) in order to get correct BCD sum need not be a 4bit parallel adder but instead it can be constructed using one Peres gate, one DPG gate and one Feynman gate similar to the existing designs which adds 011 to $S_3S_2S_1$ to produce $\Sigma_3\,\Sigma_2\,\Sigma_1$ [10, 16-17]. The Peres gate is used to add S_1 with C_{out} to produce final Σ_1 and a carry which is given to one DPG gate used as a full adder to produce final Σ_2. Then the final sum bit Σ_3 is obtained by using one Feynman gate. So the BCD sum is $\Sigma_3\,\Sigma_2\,\Sigma_1\,\Sigma_0$.The complete BCD adder is as shown in the fig.12.

In the proposed design double Peres gates are preferred since the quantum cost of a single DPG is 6[11]. The total number of garbage outputs is reduced to 10 and is the least number obtained so far compared to that obtained from other existing circuits [12-17]. Also the quantum cost of the overall circuit is minimum as compared to the other designs [12-17] because of the use of double Peres gates for the construction of adders of the BCD adder circuit.

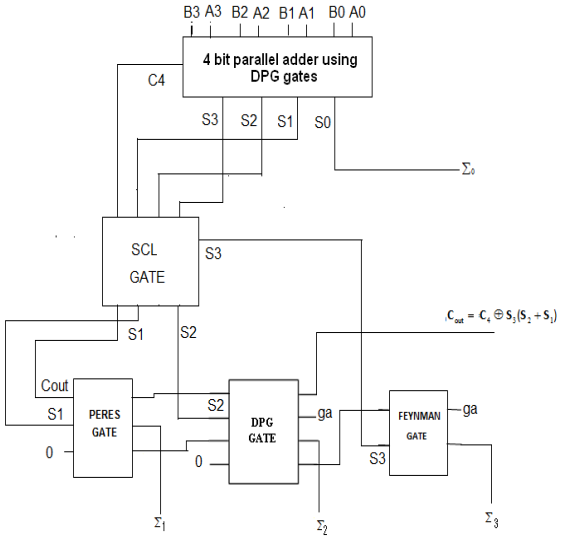


Fig.12 One digit BCD adder using reversible logic gates

b) One digit Carry skip BCD adder using reversible logic gates

The circuit can be divided into three blocks.

(i) Adder-1 and XOR-AND4 block which outputs C_{in}, C4 , Z along with S3, S2, S1 and Σ_0 shown in fig .13 and is represented in this paper as a single block shown in fig.14.

(ii) AND-OR and Correction logic circuit block which outputs $P= ZC_{in}+C_4$ and $C_{out} = P \oplus S_3 (S_2 + S_1)$ shown in fig 15.

(iii) Adder-2 block which adds 110 to S3, S2 and S1 whenever $C_{out} = 1$ and outputs the corrected BCD $\Sigma_3 \Sigma_2 \Sigma_1 \Sigma_0$ shown in fig 16.

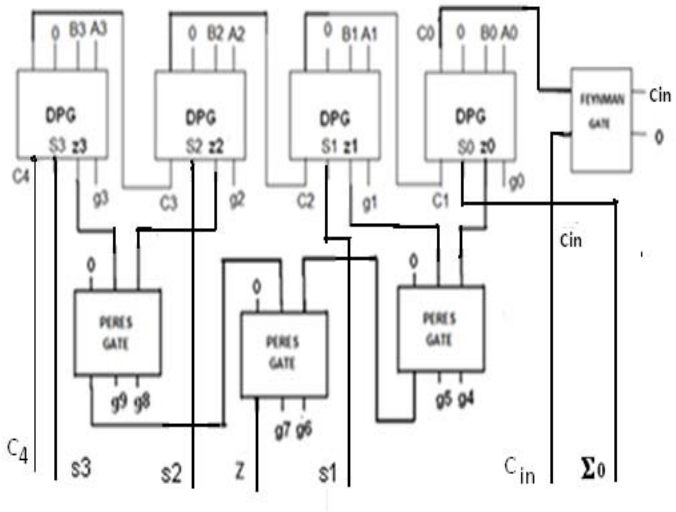


Fig 13. Adder-1 and XOR-AND4 Block

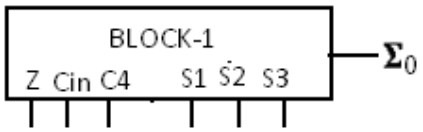


Fig.14. Adder-1 and XOR-AND4 block

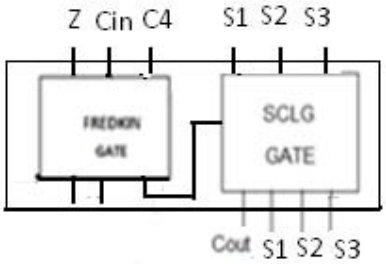


Fig.15.AND-OR and Correction logic circuit block

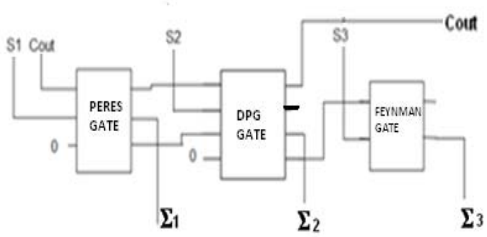


Fig.16. Adder-2 block

The proposed optimized circuit of a Carry skip BCD adder is as shown in fig 17.

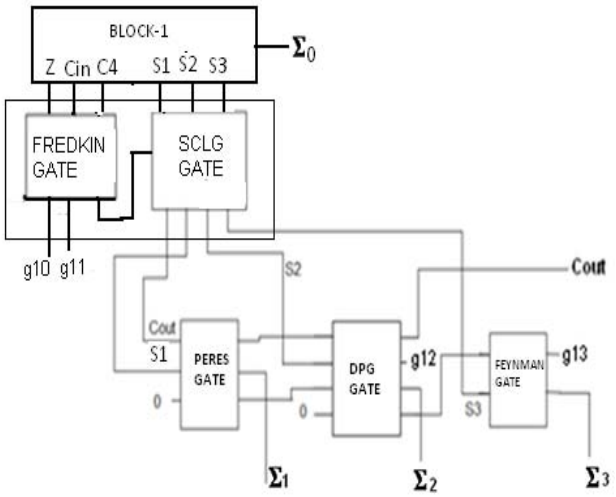


Fig.17. An Optimized Carry skip BCD adder circuit

Design details of Carry skip BCD adder:

1. Four bit parallel adder: The 4 bit parallel adder is constructed using DPG gates since it has lowest quantum cost. Also the XOR of the operand bits is readily available at one of its output which is very much required for the generation of carry propagate signal. So the total number of garbage outputs from the adder is only 4.
2. XOR gates and an AND gate: In the present circuit the function of four XOR gates is achieved without using any extra reversible gates since the XOR of the operands is available at the outputs of the DPG adder block. This produces 4 garbage outputs from the adder block. However the AND of these Z_0, Z_1, Z_2 and Z_3 is obtained by using three Peres gates. The quantum cost is reduced it is known that the quantum cost of a Peres gate is 4 [6, 19].
3. OR gate and an AND gate block: AND-OR of ZC_{in} and C_4 is obtained using a Fredkin gate which outputs $P = ZC_{in}+C_4$.
4. C_{out} generation: This is generated using a new gate SCL gate which outputs $C_{out} = P \oplus S_3 (S_2 + S_1)$ along with S_3, S2 and S1. These can be used as inputs to the next gates to correct the BCD sum.
5. Also the second adder which should add six in order to correct and convert the sum to BCD sum need not be a 4bit parallel adder but instead it can be constructed using one Peres gate, one DPG gate and one Feynman gate similar to the existing designs [16-17, 20]. The Peres gate is used to add S1 with Cout to produce final Σ_1 and a carry which is given to one DPG gate used as a full adder to produce final Σ_2. Then the final sum bit Σ_3 is obtained by using one Feynman gate. So the BCD sum is $\Sigma_3 \Sigma_2 \Sigma_1 \Sigma_0$.

VI RESULTS AND DISCUSSION

(a) BCD adder

Several researchers have proposed the 4 bit parallel adder which is constructed using different reversible full adder gates [14-17].

In [14] 3 New gates [NG] for the correction logic circuit and 8 TSG gates for the adders are used for the construction of reversible implementation of BCD adder. This reduces the number of gates but in this paper fan-out is not taken into account which when considered will increase the number of gates more than 11. This produces 22 garbage outputs with 11 constant inputs.

In [15] BCD adder is constructed using 23 reversible gates. One bit Full adder cell is realized using one NG and one PG gate which produce 2 garbage outputs. So a 4bit adder produces 8 garbage outputs and requires 8 reversible logic gates. The six correction logic is obtained using 3 TG with six garbage outputs. Also, it uses 4 FG for fan-out purpose. So the circuit of [15] uses a total of 23 reversible logic gates with 22 garbage outputs.

In [16] BCD adder is constructed using 23 reversible gates. One bit Full adder cell is realized using one NG and one NTG gate which produce 2 garbage outputs. So a 4bit adder produces 8 garbage outputs and requires 8 3*3 reversible logic gates. The six correction logic is obtained using three NG with six garbage outputs. Also it uses 4 FG far fan-out purpose. The circuit of [16] uses a total of 23 reversible logic gates with 22 garbage outputs and requires 17 constant inputs.

In [17] the BCD adder is realized using 8 HNGs along with one HNFG and one FG for fan-outs. It also uses 2 NGs, one TG and one FG for the implementation of the correction logic. This uses a total of 14 reversible gates and it produces 22 garbage outputs with 17 constant inputs in the complete circuit.

The implementation given in [18] uses two Fredkin gates and one Toffoli gate for the correction logic and also it uses a 4 bit parallel adder constructed using four TSGs. It also uses a combination of one FG, one PG and a TSG for the adder which adds the c_{out} to the sum in order to generate the final BCD sum. This implementation requires a total of 10 reversible logic gates and it produces a total number of 11 garbage outputs (including the garbage from the correction circuit) with 7 constant inputs.

The implementation given in [19] uses two Fredkin gates and one Toffoli gate for the correction logic and also it uses a 4bit parallel adder constructed using four MTSGs. It also uses a combination of one FG, one PG and a MTSG for the adder which adds the c_{out} to the sum in order to generate the final BCD sum. This implementation requires a total of 10 reversible logic gates and it produces a total number of 11 garbage outputs (including the garbage from the correction circuit) with 7 constant inputs. The advantage of using this design over that given in [18] is that the quantum cost of MTSG is less than the quantum cost of TSG [19].

The proposed design uses a DPG gate whose quantum cost is same as MTSG. However the number of reversible logic gates used in the proposed design is only 8 with number of garbage outputs 10 which is minimum as compared to the some of the designs. So the proposed design is a much optimized circuit. It uses a new gate specially designed for the correction logic circuit of a one bit BCD adder [12].

The comparative studies of different designs of BCD adders are presented in the form TABLE-I.

TABLE-I: Comparison of BCD adders

BCD adder	No of gates	No of garbages	Constant inputs	Delay
Paper(14) Without fan-out	11	22	11	10
Paper(15)	23	22	17	21
Paper(16)	23	22	17	21
Paper(17)	14	22	17	13
Paper[18]	10	10	7	10
Paper[19]	10	10	7	10
Proposed Design	**8**	**10**	**6**	**8**

(b) Carry skip BCD adder

Several designs existing in the literature are discussed and compared with the proposed design [14-17].

In [14] 3 New gates [NG] for the correction logic circuit and 8 TSG gates for the adders (for both adder-1 and adder-2 blocks) are used for the construction of reversible implementation of BCD adder. This reduces the number of gates but in this paper fan-out is not taken into account which when considered will increase the number of gates more than 15. This produces 27 garbage outputs with 11 constant inputs. The multiple fan-outs are not permitted in the synthesis of a reversible logic circuit.

The implementation given in [18] uses two Fredkin gates and one Toffoli gate for the correction logic and a 4 bit parallel adder constructed using four TSGs and a FG to fan out C_{in}. It uses a combination of one FG, one PG and a TSG for the adder-2 block which adds the c_{out} to the sum in order to generate the final BCD sum. Also to generate block generation bit P three FRGs are used. Finally to generate cout and to fan-out three sum bits another three FRGs and a TG are used. This implementation requires a total of 15 reversible logic gates and it produces a total number of 14 garbage outputs (including the garbage from the correction circuit) with 11constant inputs with a delay of 10units.

The implementation given in [19] uses two Fredkin gates and one Toffoli gate for the correction logic and also it uses a 4bit parallel adder constructed using four MTSGs. It also uses a combination of one FG, one PG and a MTSG for the adder-2 block which adds the c_{out} to the sum in order to generate the final BCD sum. Also to generate block generation bit P three FRGs are used. Finally to generate c_{out} and to fan-out three sum bits another three FRGs and a TG are used. This implementation requires a total of 15 reversible logic gates and it produces a total number of 14 garbage outputs (including the garbage from the correction circuit) with 11 constant inputs with a delay of 10 units. The advantage of using this design over that given in [18] is that the quantum cost of MTSG is less than the quantum cost of TSG [19].

The proposed design uses a DPG gate whose quantum cost is same as MTSG. Three Peres gates are used to generate Z which further reduces the quantum cost. However, the number of reversible logic gates used in the proposed design is reduced to 13 which is minimum as compared to the other existing designs. This produces 14 garbage outputs similar to the other designs. So it is observed that the proposed design is a much optimized circuit than the existing ones.

The comparative studies of various designs of carry skip BCD adders are presented in TABLE-II.

TABLE-II: Comparison of Carry skip BCD adders

Carry skip BCD adder	No of gates	No of garbages	Constant inputs	Delay
Paper(14) without fan-out	15	27	15	12
Paper(18)	15	14	11	10
Paper(19)	15	14	11	10
Proposed Design	**13**	**14**	**10**	**10**

VII CONCLUSIONS

In this paper an optimized one digit BCD adder and an optimized one digit carry skip BCD adder are presented. The design is very useful for future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of the number of reversible logic gates, the number of garbage outputs and the delay involved.

This delay is used in calculating the delay involved in an N-digit BCD adder. The delays involved in various circuits in the existing papers [14-19] are calculated on the similar lines. This delay analysis results in only approximate values as there are different types of gates used in the circuits of various papers.

The analysis of various implementations discussed is tabulated in Table-I and Table-II. It gives the comparison of the different designs in terms of the important design parameters like the number of reversible gates, number of garbage outputs, and the number of constant inputs in addition to the delay parameter. From the table it is observed that the present proposal uses the least number of gates producing the least number of garbage outputs and has the minimum gate delay compared to other design methods. Also the design uses DPG gates for the construction of adders which greatly reduces the total cost of the circuit. Because of these optimization parameters the overall cost of the circuit will be reduced. Using this one digit BCD adder, N-digit BCD adders can be constructed. The design method is definitely useful for the construction of future computers and other computational structures. Optimization of other computational circuits is under investigation as a future work.

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