

## Design and Implementation of Nanometric Fault Tolerant Reversible BCD Adder

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**Abstract:** Quantum and reversible logic circuits have found emerging attentions in nanotechnology, optical computing, quantum computing and low power CMOS design. In this paper a novel nanometric fault tolerant reversible binary coded decimal adder is proposed. To the best of our knowledge it is better than the only existing counterpart. The proposed circuit is compared with the existing counterpart in terms of number of constant inputs and garbage outputs, delay and the quantum cost. All of the parameters are improved. All the circuits have nanometric scales.

**Key words:** Quantum computing, Fault tolerant, Reversible Logic, Binary Coded Decimal, Adders, Nanotechnology Based Systems, Quantum Circuits, Quantum Gates, Nanometric Circuits.

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### INTRODUCTION

In 1961, Landauer (1961) proved that irreversible processing of information result in energy dissipation regardless of its underlying technology. It is due to the information loss. Reversible logic circuits are those circuits that do not lose information because they allow the reproduction of inputs from the observed outputs. Reversible circuits have found promising attention in nanotechnology, quantum computing, low power CMOS circuit design and optical computing. It is proved that for every bit of information that is lost during a computation,  $KT \ln 2$  Joules of energy dissipates,  $K=1.3806505 \times 10^{-23} \text{ m}^2 \text{ kg}^{-2} \text{ K}^{-1}$  (Joules/Kelvin) is the Boltzmann's constant and T is the absolute temperature at which operation is performed (BENNET, 1973). Bennet showed that zero energy dissipation would be possible if and only if the circuit made of reversible gates. A circuit is reversible if and only if for each input vector there is a unique output vector. The input vector can be uniquely recovered from the output vector. That is, there is a one-to-one mapping between its input and output vectors. Such circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs (Haghparast, 2009; Perkowski, 2001; Perkowski, 2001; Haghparast, 2011; Kerntopf, 2004; Mohammadi, 2009). Thus in the future the reversibility will become an essential and vital property of the circuits.

Synthesis of reversible logic circuits differs from the irreversible one (Gupta, 2006). In the past decade some reversible logic circuit synthesis methods are proposed (Gupta, 2006 ; Maslov, 2003). In reversible logic circuits feedback and fan-out are forbidden. In addition for each input vector there should be a unique output vector. There are some important factors in designing reversible logic circuits such as the number of garbage outputs, the number of constant inputs, hardware complexity and the quantum cost (QC). We should try to minimize them (Gupta, 2006; Maslov, 2005; Haghparast, 2007; Haghparast, 2008; Haghparast, 2008; Haghparast, 2006).

Constant inputs refer to the input lines that are either set to zero (0) or one (1) in the circuit's input side. Garbage outputs refer to the outputs that are not used as primary outputs. Hardware complexity refers to the number of gates (NOT, AND and EXOR gate) used to synthesize the function of the circuit. The quantum cost (QC) of a reversible circuit is defined as the number of  $1 \times 1$  or  $2 \times 2$  reversible or quantum logic gates that are needed to realize the circuit. For instance, the QC of FG, Toffoli, Fredkin, NFT, Peres and F2G gates are 1, 5, 5, 5, 4 and 2, respectively.

In addition it is to be noted that design of fault-tolerant reversible circuit is also much more difficult than a conventional logic circuit (Haghparast, 2008; Haghparast, 2008; Haghparast, 2006).

If a system is made up of fault tolerant components, then it will be able to continue its operation properly when the failure occurs in some of its components. The detection and correction of faults in such fault tolerant systems are much easier. We can achieve fault tolerance in many systems by using parity bits. Thus, parity preserving reversible circuit design will be very important for development of fault tolerant reversible systems in nanotechnology which is an emerging technology (Saiful 2008).

In this paper we propose a novel nanometric fault tolerant reversible BCD adder. All the scales are in the nanometric area. This design is better than the existing design in (Saiful 2008) in the sense of above mentioned complexity factors.

The organization of the paper is as follows: Section 2 covers the basic concepts including reversible logic gates and circuits, parity preserving reversible gates and circuits, and BCD adder.

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Our proposed fault tolerant reversible BCD adder is presented in section 3. Comparison of the proposed circuit with the existing design is also presented in section 4. Conclusions and references are in sections 5 and 6, respectively.

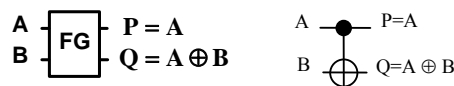
## 2. Background:

This section includes some background information about reversible logic gates and circuits, fault tolerant reversible gates, existing fault tolerant reversible BCD adder and necessary blocks to construct our design.

### 2.1 Reversible Gates:

A gate or a circuit is reversible if and only if there is a one-to-one mapping between its inputs and outputs (Haghparsat, 2007; Haghparsat, 2008; Haghparsat, 2008; Haghparsat, 2006; Saiful, 2008). Reversible logic gates can be implemented in various technologies such as CMOS logic, optical logic, quantum and nanotechnology.

Feynman (1985) gate is a 2\*2 reversible gate which is shown in Fig. 1. Its QC is 1. Reversible Toffoli (1980) gate which is depicted in Fig. 2 is 3\*3 reversible gate. The Toffoli gate is universal, i.e. any logical reversible circuit can be implemented using this gates. Its QC is 5.

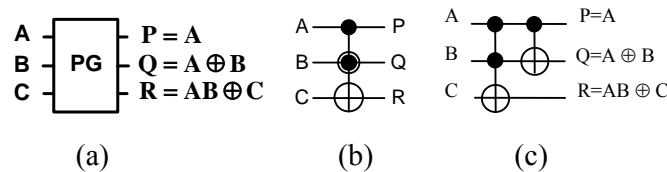


**Fig. 1:** Two symbols of Feynman gate.



**Fig. 2:** Symbol of Toffoli gate and its functionality.

Peres gate (1985) also known as New Toffoli gate (NTG), can be constructed by one Toffoli and one Feynman gate is a 3\*3 reversible logic gate. The Peres gate is shown in Fig. 3. Its QC is 4.



**Fig. 3:** Peres gate: (a) symbol and functionality, (b) The symbol used in this paper (c) equivalent circuit.

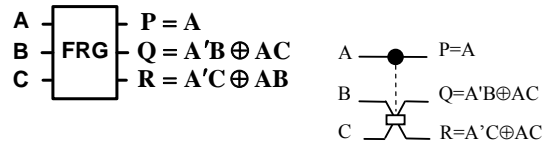
### 2-2 Parity Preserving Reversible Gates and Circuits:

Among reversible logic gates (or circuits), those gates (or circuits) which have the equal input parity and output parity are “parity preserving reversible gates (or circuits)”. Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems. Therefore it is important to construct parity preserving reversible gates and circuits.

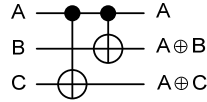
There exist a few parity-preserving reversible gates. The Fredkin (1982) gate (FRG) depicted in Fig. 4, the F2G (Parhami, 2006) gate depicted in Fig. 5, and the NFT gate depicted in Fig 6 are parity-preserving 3\*3 reversible gates. These gates are parity preserving gates because their input parity  $A \oplus B \oplus C$  is the same as their output parity  $P \oplus Q \oplus R$ .

Fredkin (1982) gate is a 3\*3 reversible gate. It is a universal gate, i.e. any logical reversible circuit can be implemented using this gate. The Fredkin gate acts as a controlled cross switch. If the control input of a Fredkin gate (A input) is ‘0’, then its target outputs, P and Q, are the same as the corresponding inputs, B and C, respectively. If the control input is ‘1’, then the target outputs are swapped values of their corresponding inputs. Its QC is 5.

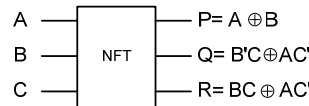
F2G gate is also a fault tolerant reversible gate. Its QC is only 2. NFT gate is another useful fault tolerant reversible gate which is universal. Its QC is only 5. The IG gate is also a 4\*4 parity preserving reversible gate. The IG gate is depicted in Fig.7. Its QC is 7.



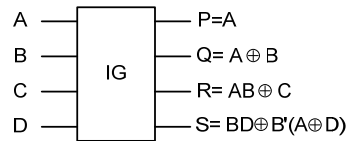
**Fig. 4:** Parity Preserving Reversible Fredkin gate.



**Fig. 5:** Parity Preserving Reversible F2G gate.



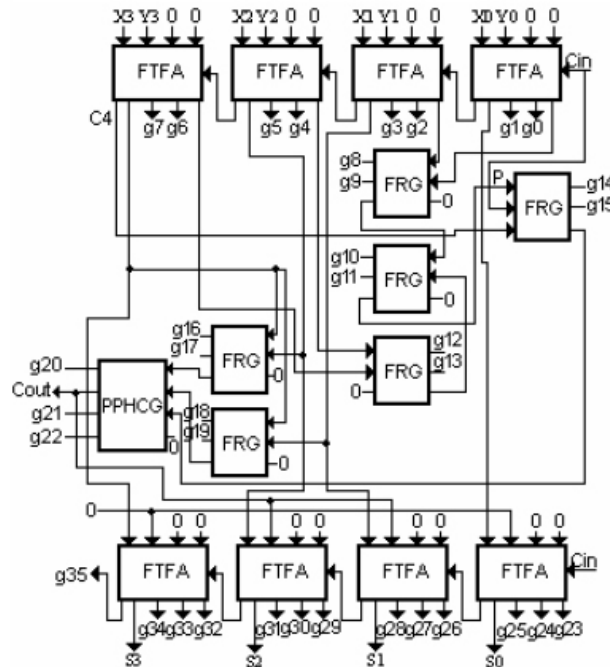
**Fig. 6:** Parity-preserving reversible NFT gate.



**Fig. 7:** Parity-preserving reversible IG gate.

### 2.3 Existing Fault Tolerant Reversible BCD Adder:

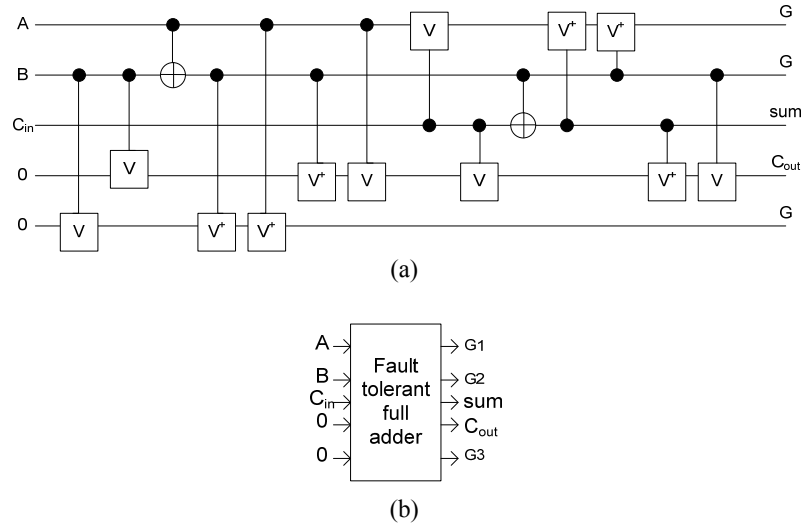
To the best of our knowledge there is only a fault tolerant reversible BCD adder in (Saiful, 2008). It is depicted in Fig. 8. It includes two four-bit fault tolerant reversible full adder blocks, six Fredkin gates and a PPHCG gate. The QC of PPHCG is only 6. This design produces 40 garbage outputs. It also requires 24 constant inputs. The quantum cost of this circuit is 148.



**Fig. 8:** Existing fault tolerant reversible BCD adder.

#### 2.4 Four Bit Fault Tolerant Reversible Full Adder:

In this paper we use the existing fault tolerant reversible full adder in (Dastan, 2011) to construct a four bit fault tolerant reversible full adder. The existing fault tolerant reversible full adder has a QC of only 14. It has two constant inputs and produces only three garbage outputs. The existing fault tolerant reversible full adder in (Dastan, 2011) is depicted in Fig. 9. To construct the four bit fault tolerant reversible full adder we need 4 fault tolerant reversible full adders.



**Fig. 9:** Fault tolerant reversible full adder in (Dastan, 2011) (a) Quantum Representation. (b) Block diagram.

#### 4. Our Proposed Fault Tolerant Reversible BCD Adder:

Our proposed parity preserving reversible BCD adder is depicted in Fig. 10. It includes two 4-bit fault tolerant reversible full adder blocks, three NFT gates and two F2G gates. The QC of the proposed circuit is 131. This design produces 29 garbage outputs. It also requires 24 constant inputs. To compute the hardware complexity of the proposed design, Let:

$\alpha$  = A two input EX-OR gate calculation

$\beta$  = A two input AND gate calculation

$\delta$  = A NOT calculation

T= Total logical calculation

Thus the hardware complexity of the proposed circuit is  $T=80\alpha+57\beta+22\delta$ .

#### 5. Evaluation of the Proposed Fault Tolerant Reversible BCD Adder:

Our proposed parity preserving reversible BCD adder performs better than the existing circuit presented in (Saiful, 2008). An experimental result will comprehend it clearly. Table 1 compares the proposed reversible circuit with the existing counterpart. Our proposed circuit is better than (Saiful, 2008) in term of complexity:

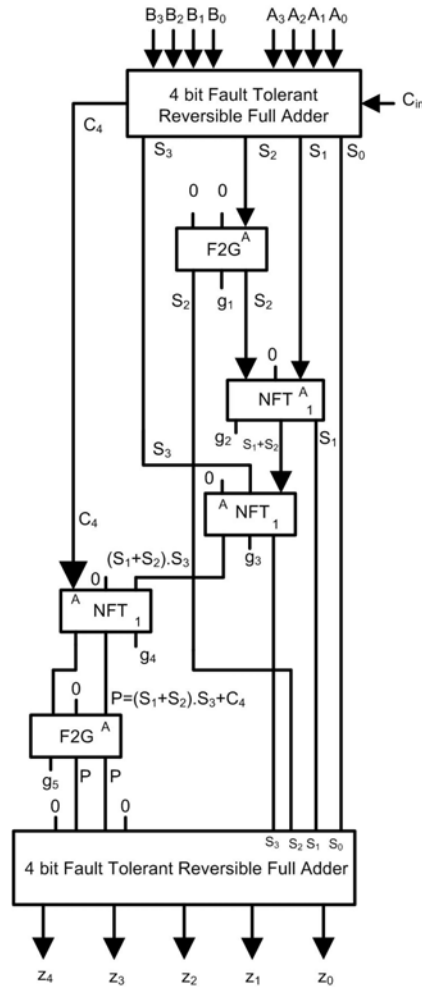
For (Saiful, 2008):  $T=84\alpha+72\beta+28\delta$

For our proposed circuit:  $T=80\alpha+57\beta+22\delta$

Thus, the propounded parity-preserving reversible circuit requires less logical calculations than (Saiful, 2008). One of the other major constraints in reversible logic is to minimize the quantum cost of the circuit. The QC of the proposed design is 131. The QC of the existing design in (Saiful, 2008) is 148. Thus we can state that the proposed circuit is better than (Saiful, 2008) in term of quantum cost. Another significant criterion in designing a reversible circuit is to lessen number of constant inputs. A heavy price is paid for every constant input bit. The proposed reversible circuit has 29 constant inputs. The design in (Saiful, 2008) has 40 constant inputs. Thus, we can state that our design is better than (Saiful, 2008) in term of number of constant inputs.

**Table 1:** Specifications of The proposed fault tolerant reversible BCD adders in this work and the only existing counterpart.

Design	No. Gin	No. Gout	QC	Hardware Complexity
This Work	24	29	131	$80\alpha+57\beta+22\delta$
Existing [17]	24	40	148	$84\alpha+72\beta+28\delta$
Improvement	-	27.5%	11.48%	-



**Fig. 10:** Our proposed fault tolerant reversible BCD adder.

## 6. Conclusion:

In this paper we proposed a novel fault tolerant reversible BCD adder. It is much better than the existing counterpart. The proposed circuit is compared with the existing circuit in terms of the number of constant inputs, number of garbage outputs, hardware complexity and quantum cost (QC). Table 1 compares the proposed circuit with the existing circuit. All the scales are in the nanometric area. The proposed circuit can be used in the design of fault tolerant quantum computers.

## Nomenclatures:

Exclusive OR:	$\oplus$
Feynman Double Gate:	F2G
Feynman Gate:	FG
Fredkin Gate:	FRG
Islam Gate:	IG
New Fault Tolerant Gate:	NFT
Peres Gate:	PG
Quantum Cost:	QC
Toffoli Gate:	TG

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