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Investigation of veritcal graded channel doping in nanoscale fully-depleted SOI-MOSFET

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ABSTRACT

For achieving reliable transistor, we investigate an amended channel doping (ACD) engineering which improves the electrical and thermal performances of fully-depleted silicon-on-insulator (SOI) MOSFET. We have called the proposed structure with the amended channel doping engineering as ACD-SOI structure and compared it with a conventional fully-depleted SOI MOSFET (C-SOI) with uniform doping distribution using 2-D ATLAS simulator. The amended channel doping is a vertical graded doping that is distributed from the surface of structure with high doping density to the bottom of channel, near the buried oxide, with low doping density. Short channel effects (SCEs) and leakage current suppress due to high barrier height near the source region and electric field modification in the ACD-SOI in comparison with the C-SOI structure. Furthermore, by lower electric field and electron temperature near the drain region that is the place of hot carrier generation, we except the improvement of reliability and gate induced drain lowering (GIDL) in the proposed structure. Undesirable Self heating effect (SHE) that become a critical challenge for SOI MOSFETs is alleviated in the ACD-SOI structure because of utilizing low doping density near the buried oxide. Thus, refer to accessible results, the ACD-SOI structure with graded distribution in vertical direction is a reliable device especially in low power and high temperature applications.

1. Introduction

As MOSFETs dimensions are pushing device scaling into sub-50 nm regime, reliability and short channel effects (SCEs) issues have become critical challenges [1,2]. MOSFETs dimensions shrinking leads to scale the conventional gate oxide thickness that increases the gate leakage current [1,2]. So, alternative approaches in term of channel engineering utilizing became a critical part of device design to alleviate these concerns [1–10]. Hot electron degradation and SCEs affairs including threshold voltage roll off, drain induced barrier lowering (DIBL) suppression are some of the critical issues that can be addressed with proper channel doping profile design [3–10]. SCEs can be mainly referenced to the DIBL effect that result in threshold voltage alleviation as the channel length decreases. SCEs reliability issues such as device characteristic dependence on channel length like threshold voltage leads to device characteristics scattering because of the variation of gate length produced during the fabrication process [3,4,6].

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Furthermore, SCEs leads to gate voltage controllability degradation to drain current which causes off current increment [5–7,9]. In the weak inversion regime, at source to channel junction is a potential barrier that control of its height is an important issue for leakage current improvement [4–7]. The potential barrier height for channel carriers should ideally be controlled by the gate voltage. SCEs especially DIBL effect are happened due to impact of drain electric field because of high drain voltage application when the potential barrier height for channel carriers at the edge of the source decreases. The result of this reduction is the increment of injected carriers into the channel from the source that leads to the off current enlargement. So, the drain current is controlled not only by the gate voltage, but also by the drain voltage that is a critical challenge and can be solved by proper channel doping [5,8–10]. Some efforts for channel engineering have considered such as halo and pocket implant that improve the SCEs and suppressed high leakage current of short channel devices [5,8–10]. One of the primary reasons of short channel device performance degradation is the drain electric field enlargement in the channel region. The reliability problems have also been more severe particularly in the high electric field near the drain that poses a limit on the device performance including large gate current, substrate current, and so on [2,4–7,10]. In short channel devices, according to the large electric field, carriers can gain enough energy for trapping into the gate oxide [5]. Some ways have proposed for reliability and hot carrier degradation issues in scaled transistors [4–7].

Generally, SCEs can be well suppressed by utilizing thin-film SOI MOSFETs compared to bulk MOSFETs, because thin-film SOI MOSFETs have a larger immunity against to the SCEs in comparison with the bulk MOSFETs [11]. Moreover, SOI MOSFETs brings in new reliability challenge that is not considered in the conventional bulk MOSFETs because of the buried oxide presence which acts as a barrier for thermal releases and explicit as self-heating effect (SHE). Many innovative structures have considered for suppression of self-heating effect and transistors temperature reduction [12–19]. The majority of them have worked on the buried insulator shape like the thickness of it, replacing SiO_2 with the other materials with better thermal conductance, and so on [12–17]. Furthermore, in the fully-depleted SOI-MOSFET, higher device temperature is achieved compared to the partially-depleted SOI-MOSFET [19], because the drain current increases with silicon-on-insulator layer reduction. So it will be very beneficial if we can reduce the device temperature with channel doping engineering without any changes in the buried insulator.

In this paper, we investigate a channel doping engineering that improves electrical and thermal performances of the scaled fully-depleted SOI-MOSFETs. The improvements are included SCEs, hot electron degradation, self-heating, leakage current, and gate induced drain lowering (GIDL) suppression. Graded doping distribution in the vertical direction that starts with high doping density in the surface of the structure and goes graded to the bottom of the channel, near the buried oxide, with low doping density is employed in the channel. Based on the above idea, the potential profile modification helps for improving SCEs and leakage current. The barrier height increment aids for lower injected carriers into the channel and makes less leakage current in weak inversion regime. On the other hand, with lower peak of the electric field especially near the drain region, fewer carriers get energy for trapped into the gate oxide. Furthermore, by electric field maximum value reduction, SCEs, GIDL, and hot electron degradation suppression is expectable. The proposed device structure called amended channel doping (ACD) engineering with vertical graded doping channel fully-depleted silicon-on-insulator (ACD-SOI). Using two-dimensional simulation [20], we have compared the ACD-SOI structure with the conventional fully-depleted SOI-MOSFET with uniform doping in the channel (C-SOI). Moreover, by employing the amended doping distribution in the channel, low doping density is used in the bottom of the channel, near the buried oxide region compared to the C-SOI structure that leads to maximum lattice temperature reduction because of higher mobility without any changes in the buried oxide layer. Also, we have examined the effects of doping parameters in electrical and thermal performance of the device.

2. ACD-SOI structure and simulation

The implemented ACD-SOI structure is shown in Fig. 1. A p-type silicon doping is graded vertically in the proposed structure from high to low doping densities from the structure surface to the bottom of the channel as shown in Fig. 2. Also, the C-SOI structure is doped at 1×10^{17} cm^{-3} uniformly that is shown in Fig. 2. For investigation of the proposed doping distribution on the electrical and thermal performances, we simulated two models of it as Model A and Model B. We have named high and low doping densities of the ACD-SOI as N_H and N_L, respectively. The N_H and N_L of the Model A is 5×10^{18} cm^{-3} and 5×10^{15} cm^{-3} while in the Model B is 1×10^{19} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The slope of doping distribution is named as S that is higher for the Model B compared with the Model A. We have compared the ACD-SOI structure with that C-SOI with equivalent parameters except channel doping distribution profile. The doping in the n^+ Source/Drain is kept at 1×10^{20} cm^{-3}. Note that the typical values of the silicon thin film, gate oxide and channel length are 10, 1, and 35 nm, respectively.

The 2-D ATLAS simulator from Silvaco is used to evaluate numerical device characteristics [20]. It is imperative to use accurate models in order to achieve realistic results. Because of SHE consideration, we utilized lattice temperature model in our simulations that is Lat.temp. Some equations in term of Poisson's equation, current continuity equation, and heat equation are solved in a completely coupled manner for lattice temperature obtaining. Also for SHE consideration, we utilized thermo contact and fixed the boundary condition of the heat flow at the bottom interface of the silicon substrate in 300 K. It is worthy to note that the isothermal and non-isothermal behaviors deviation in the simulations is referring to the SHE. In addition to SHE model we utilized some other models such as Impact Selb model for impact ionization because of reliability consideration. In short channel devices, the electric field becomes enlarge that leads to extremely higher temperature of the carriers compared to the ambient temperature that is invalid [4–7]. We use the hydrodynamic model to simulate the temperature effect and the lateral electric field-dependent mobility and concentration dependent mobility models. Also energy

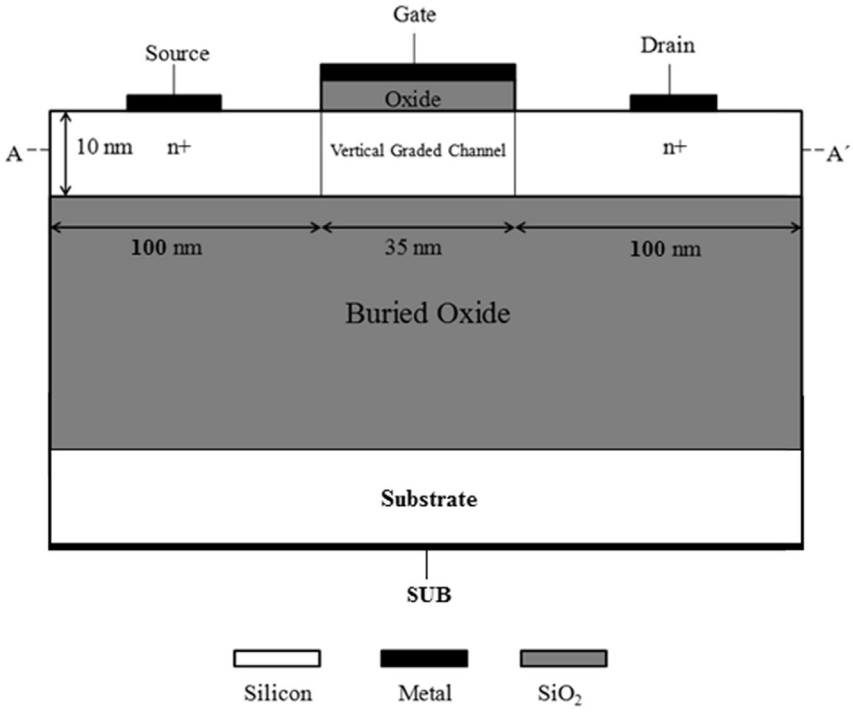

Fig. 1. Cross section of the ACD-SOI structure.

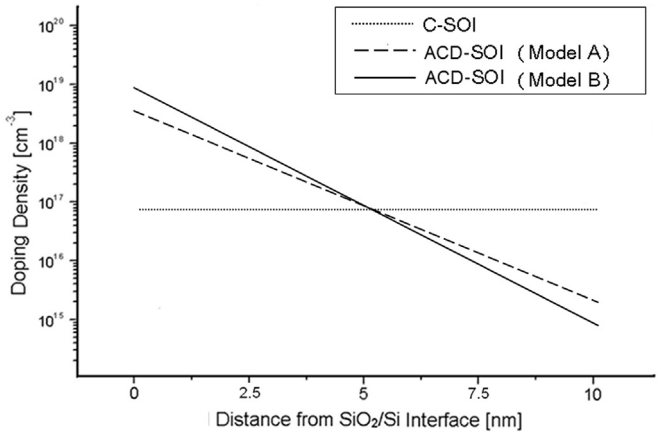

Fig. 2. Channel doping distribution profiles for the ACD-SOI and C-SOI structures.

balance equation is active in addition to the conventional drift models, in ATLAS simulator [20] for improved describing the drain current characteristics and prediction of the short-channel device behavior.

The relaxation times are extremely important as they determine the time constant for the rate of energy exchange. Therefore, we have used the accurate model and the parameter values for the energy relaxation time model for silicon [21,22].

We also propose a process flow for the fabrication of the ACD-SOI structure. The process starts with a P-type silicon substrate at stage 1. Then, the oxygen ion implantation is done to form a buried oxide at stage 2. Stage 3 includes the p-type channel and the solid state diffusion for fabrication of the graded p-type silicon channel [23]. Afterward in stage 4, the phosphorus ion implantation is performed to constitute active area regions (source/drain regions). The final stage includes the formation of the gate oxide and metallization as same as those done for a conventional SOI.

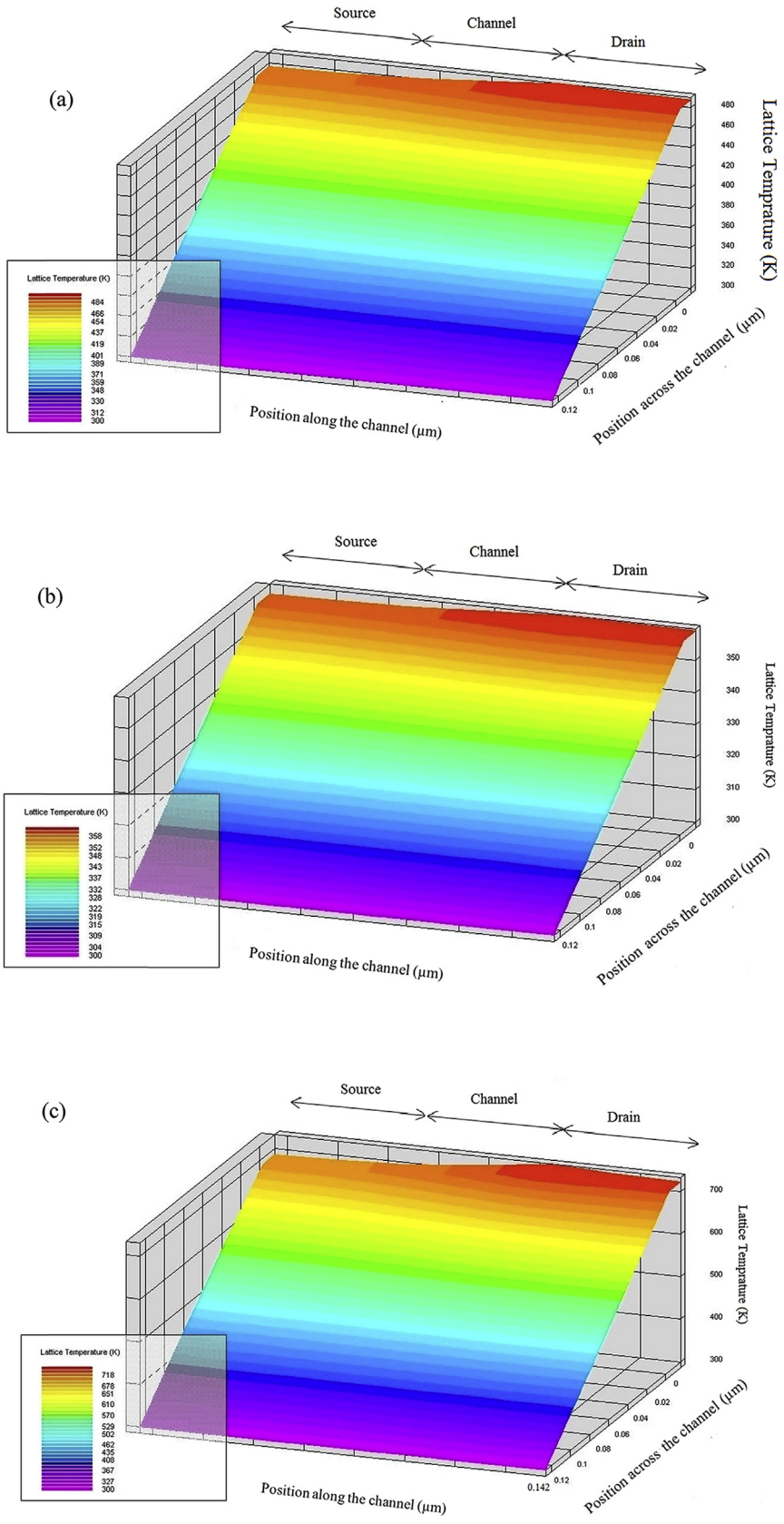

Fig. 3. Temperature Distribution for (a) ACD-SOI (Model A) (b) ACD-SOI (Model B) and (c) C-SOI structures at $V_G = 0.55$ V and $V_D = 2$ V.

3. Results and discussion

3.1. Self-heating effect suppression

As already mentioned in the introduction section, SOI-MOSFETs suffer from the SHE that is because of buried oxide which acts as a barrier for heat dissipation. In the ACD-SOI structure without any changes in the buried insulator, we access to lower lattice temperature due to the low doping density near the buried insulator. Fig. 3 shows the temperature distribution of the ACD-SOI and C-SOI structures at $V_G = 0.55$ V and $V_D = 2$ V. For the ACD-SOI structure in both the models the lattice temperatures are less than that achieved in the C-SOI structure is achieved. Especially for the Model B we access noticeable reduction of the temperature that improves the SOI performances in high temperature applications. Furthermore, Fig. 4 demonstrates the maximum lattice temperature versus the drain voltage. As can be seen from the figure, with drain bias increment, higher temperature is achieved. For example 490 K and 359 K for the Model A and Model B, respectively in the proposed structure show 33% and 50% maximum temperature reduction of models, respectively, compared to the C-SOI structure that has 731 K maximum temperature at $V_D = 1.5$ V. Significant reduction of temperature especially in the Model B of the ACD-SOI structure without any changes in the buried insulator is very interesting.

3.2. Hot electron degradation improvement

In this section, we demonstrate by employing vertical graded doping in the channel in the ACD-SOI structure, reliability is improved. It is common practice to simulate the electric field and electron temperature profiles in the structure for proofing of the hot electron degradation suppression. By the reduction of the electric filed peak and maximum electron temperature values, near the drain junction that is the place of hot electron generation, we can expect reliability improvement. Fig. 5 shows the electric field of the both the structures along the AA' cutline that is located at 5 nm from the structure surface which is the cross point of uniform and vertical graded doping in the conventional and proposed structure, respectively. Near the drain region is the place of hot electron generation due to electric field peak. High electric filed stimulated the channel carriers for trapping in the gate oxide. So as can be seen from the figure, in the ACD-SOI structure, the lower peak of electric field is achieved that leads to lower accelerate of carriers for trapping in the gate oxide and causes reliability improvement. As we mentioned before, we can understand hot electron degradation suppression from electron temperature reduction especially in maximum value of it. The maximum electron temperature is near the drain region because of the electric field peak presence. However, we can expect the reliability improvement if this parameter be lower. The maximum value of the electron temperature as shown in Fig. 6 for the Model A and Model B of the ACD-SOI structure is 3963 K and 3893 K, respectively while for the C-SOI structure is 4226 K. It is common practice that we measure gate and substrate current for reliability suppression. So Fig. 7 shows the gate current of both the structures at $V_G = 2$ V and $V_D = 2$ V. We simulated in high drain and gate voltages, because of hot electron generation confidence. As can be seen from the figure, gate current of the ACD-SOI structure in both models reduces significantly. The main reason for this circumstance is decrement of the electric field peak. For having an estimation of gate current reduction, Fig. 7 shows 79% and 90% alleviation of the Model A and Model B gate current, respectively in comparison with the C-SOI structure at $V_G = 2$ V. On the other hand a noticeable reduction of the substrate current in the ACD-SOI structure is achieved as can be seen in Fig. 8. For example, the substrate current peak of the Model A and Model B in the ACD-SOI structure at $V_G = 1.5$ V is 2.1 and 1.8 μA/μm, respectively while in the C-SOI structure is 3.2 μA/μm that shows 34% and 43% reduction of this characteristic and reliability improvement. Generally, we prove that by a proper doping distribution in the channel we can achieve to the reliable device that alleviate hot carrier degradation and perform like an ideal SOI MOSFET.

3.3. Leakage current reduction

One of the chief reasons of leakage current enlargement in short channel devices is SCEs. The SCEs that happened due to source and drain depletion region penetration into the channel causes channel length seems less than actual length and this phenomenon leads to DIBL and leakage current increment. So, we should suppress the SCE including DIBL and threshold voltage roll off. On the other hand, potential barrier height growth with channel engineering ways can aid for leakage current alleviation. Because, high barrier height result in less injected carriers into the channel from the source region in weak inversion regime that lead to a leakage current reduction. Fig. 9 shows the leakage current of the ACD-SOI structure in both models and C-SOI structure. As can be seen from the figure noticeable reduction of the leakage current is achieved. Furthermore, it is interesting that by employing high to low vertical graded doping in the channel we can access to the GIDL improvement in addition to the lower leakage current as shown in Fig. 9. GIDL is due to the high electric field effect of the MOSFETs at the drain junction. In the ACD-SOI structure we have less value of the electric field peak near the drain region end of the channel as shown in Fig. 5. The lower electric filed leads to GIDL suppression. On the other hand, significant less gate current of the ACD-SOI structure compared to the C-SOI as shown in Fig. 7 is an excellent proof for GIDL improvement in the proposed structure. Fig. 9 shows that C-SOI structure has a clear GIDL effect but in the ACD-SOI structure especially for the Model B, there is no significant GIDL. As it mentioned before the barrier height increment is helpful for the leakage current reduction. As can be seen from Fig. 10, potential barrier height of the ACD and C SOI structures is simulated at weak inversion regime along the AA' cutline. Higher potential barrier height of the ACD-SOI structure proved the leakage current reduction of

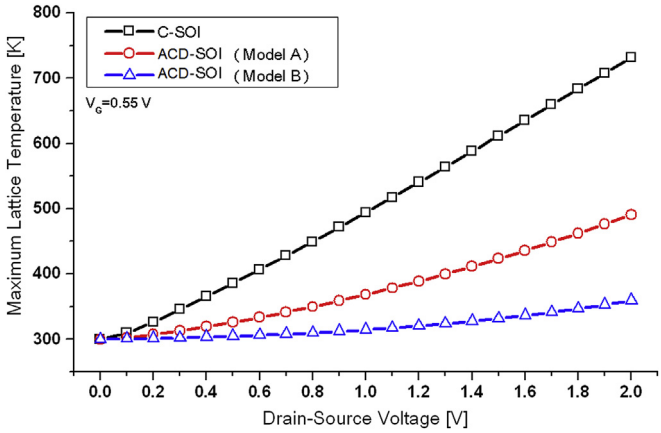

Fig. 4. Maximum lattice temperature versus V_{DS} for the ACD-SOI and C-SOI structures in $V_G = 0.55$ V.

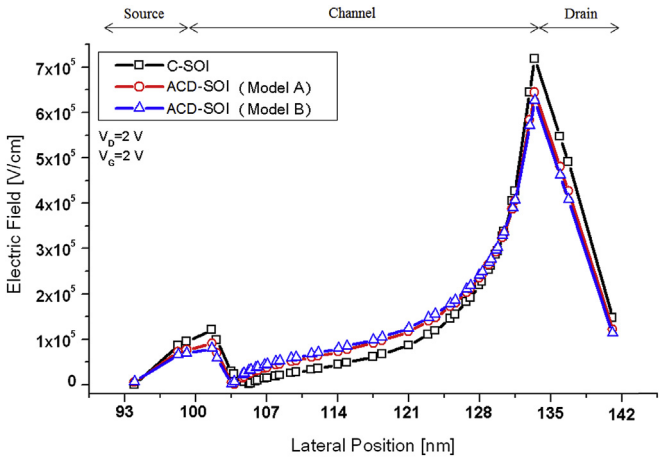

Fig. 5. Horizontal electric field of the ACD-SOI, and C-SOI structures along the AA′ cutline at $V_G = 2$ V and $V_D = 2$ V.

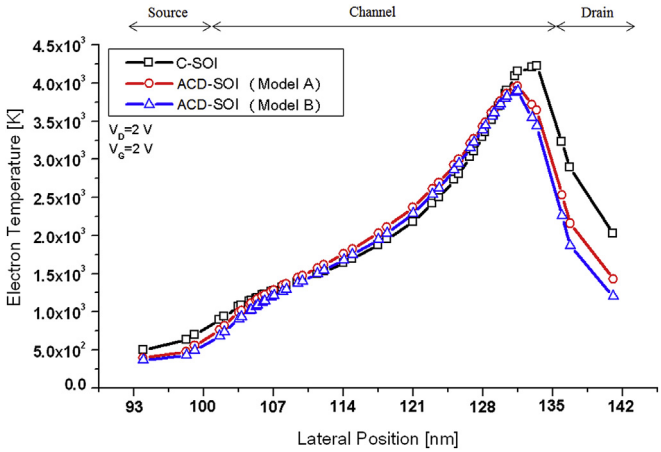

Fig. 6. Electron temperature profiles along the AA′ cutline for the ACD-SOI and C-SOI structures in $V_G = 2$ V and $V_D = 2$ V.

the proposed structure as shown in Fig. 9. When carriers forbid for injection into the channel and fewer carriers can go there because of the high potential barrier height, we can expect lower leakage current of the novel structure. Furthermore,

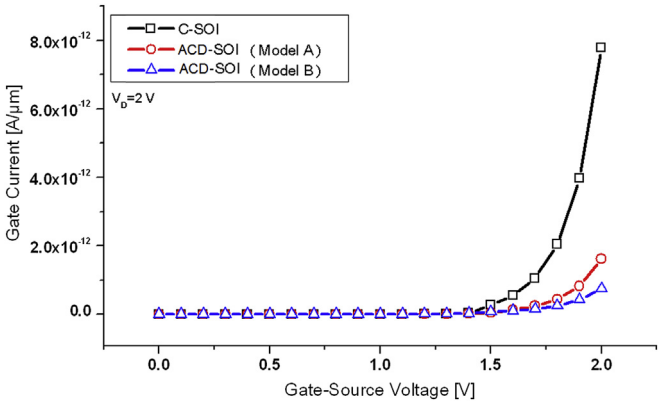

Fig. 7. Gate current versus gate-source voltage for the ACD-SOI and C-SOI structures in $V_D = 2$ V.

according to the vertical distribution of the proposed structure, we demonstrate potential in vertical direction like the method of doping distribution in Fig. 11. It is very grateful that in this direction high potential barrier height of the ACD-SOI structure compared to the C-SOI structure is achieved. As can be seen from the figure there is no clear barrier height for the C-SOI structure while for the ACD-SOI, we have a significant potential barrier height. So, in addition to the horizontal high barrier height, we have a vertical high barrier height that helped for leakage current alleviation.

DIBL is an effect that happened due to an electric field in high drain voltage applications. Charge sharing and source/drain penetration into the channel make less barrier height that called DIBL. So we should decrease the interaction of the source and drain depletion region in order to SCEs alleviation. Fig. 12 shows DIBL profile of the proposed and conventional structures versus the channel length variation. As can be seen from the figure, lower DIBL of the ACD-SOI structure is achieved because of the vertical graded doping distribution. In addition to the lower DIBL, less dependence of it on channel length variation for the ACD-SOI structure aid for leakage current reduction.

DIBL has a detrimental effect because of channel barriers lowering. This leads to the threshold voltage reduction that is out of our interest. Because this reduction of threshold voltage is fake and make with drain voltage not only by gate voltage because of the DIBL. So the increment of the threshold voltage in Fig. 13 for the ACD-SOI structure is due to the SCEs improvement. On the other hand, in the short channel devices as we reduce the channel length, the threshold voltage gets decrease because of the mentioned DIBL effect. So we should alleviate this dependence and make a flatter line of threshold voltage dependence on the channel length variation. As can be seen from Fig. 13, poor dependence of the ACD-SOI structure threshold voltage on channel length changes for both models is access. So, we get to the SCEs improvement in the ACD-SOI structure by channel doping engineering.

One of the important parameters of a transistor is on-off current ratio (I_{on}/I_{off}) that assign with the on and off change. In the ACD-SOI structure due to the significant alleviation of the off current, we have a large value of the I_{on}/I_{off}. As can be seen from Fig. 14, the I_{on}/I_{off} is nearly three orders of magnitude in the ACD-SOI (Model B) structure larger than it at the C-SOI in 35 nm of the channel length. Furthermore, by channel length reduction, the I_{on}/I_{off} become lower, but the important fact is the variation of this parameter versus the channel length should be very poor as can be seen from Fig. 14 for the ACD-SOI structure. For example in the 20 nm of the channel length there is between three to five orders of the I_{on}/I_{off} magnitude in the ACD-SOI structure in comparison with the C-SOI.

4. Design consideration of the ACD-SOI

In this section, we studied the doping distribution slope on the electrical and thermal characteristics of the ACD-SOI structure. For having symmetric shape for doping distribution, higher doping density in the surface of the structure (N_H) leads to lower doping density in the bottom of the channel near the buried oxide (N_L) and causes higher slope (S). Thus, we have calculated some characteristics refer to the electrical and thermal performances. For doping distribution slope impact on the SCEs and leakage current, we demonstrated DIBL and I_{on}/I_{off} and for reliability changes with slope, the maximum electron temperature is calculated. The mentioned characteristics are for electrical characteristics variation with doping distribution slope. On the other hand, maximum lattice temperature changes with various slopes is demonstrated for the SHE investigated. As can be seen from Table 1, by the higher slope of the doping distribution, less maximum lattice temperature is achieved. Because the higher slope of the doping density distribution means less doping density near the buried oxide layer that causes lower maximum lattice temperature. As can be seen in Figs. 5 and 6, Model B of the ACD-SOI structure has lower electric field peak and maximum electron temperature compared to the Model A. Model B has more slope than that is in the Model B. We investigated the maximum electron temperature for many doping distribution slopes and we reach to the define result that the high slope of doping density distribution leads to lower peak of the electron temperature which causes reliability improvement.

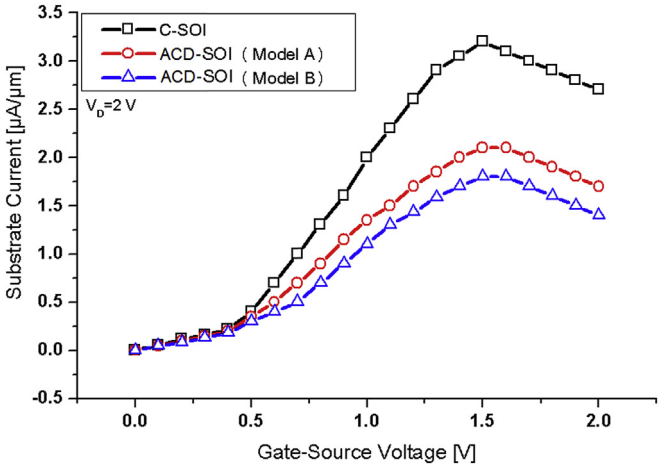

Fig. 8. Substrate current versus gate-source voltage for the ACD-SOI and C-SOI structures in $V_D = 2$ V.

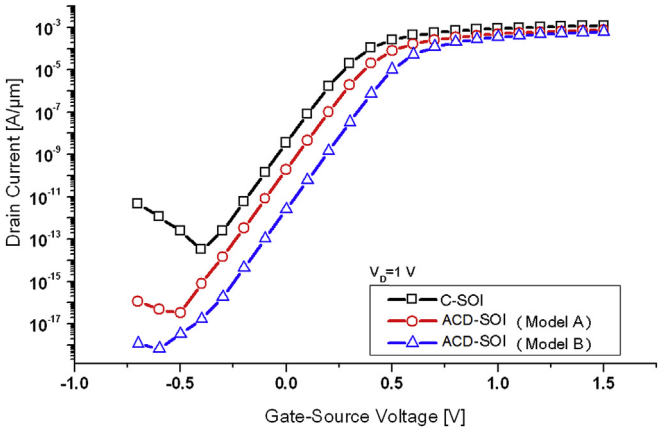

Fig. 9. I_D versus V_{GS} for the ACD-SOI and C-SOI structures at $V_D = 1$ V.

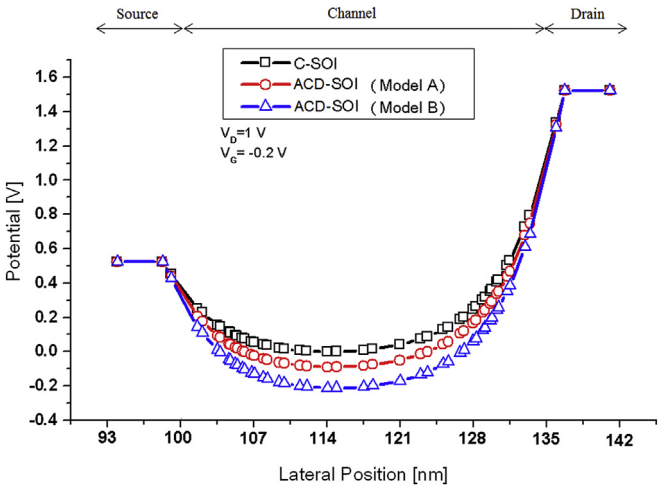

Fig. 10. Potential profiles of the ACD-SOI and C-SOI structures along the AA′ cutline at $V_G = -0.2$ V and $V_D = 1$ V.

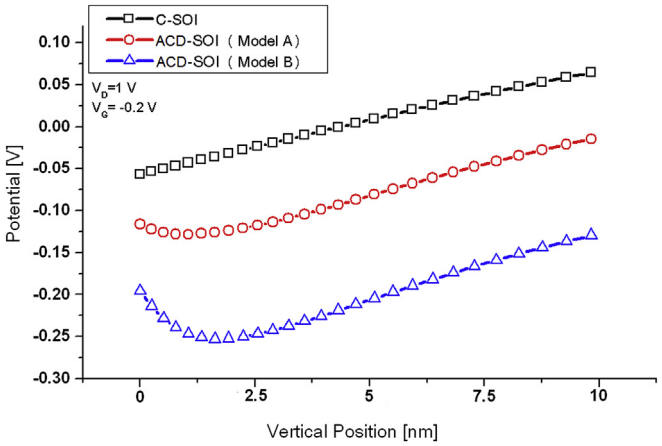

Fig. 11. Vertical potential profiles in the channel for the ACD-SOI and C-SOI structures at $V_G = -0.2$ V and $V_D = 1$ V.

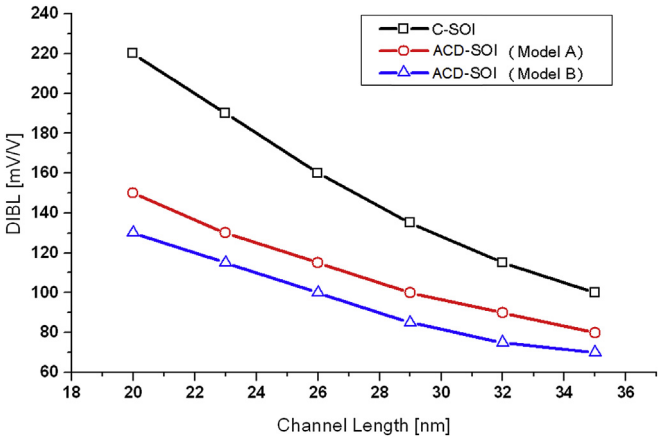

Fig. 12. DIBL of the ACD-SOI and C-SOI structures versus channel length up to 20 nm.

In Table 2, we have investigated Effective electron mobility, DIBL and I_{on}/I_{off} for various doping parameters in the channel for their effect on the SCEs and the leakage current mechanism. As we proved before in the ACD-SOI structure due to the vertical graded doping distribution the DIBL is decreased. The reduction of the effective electron mobility and the DIBL can be

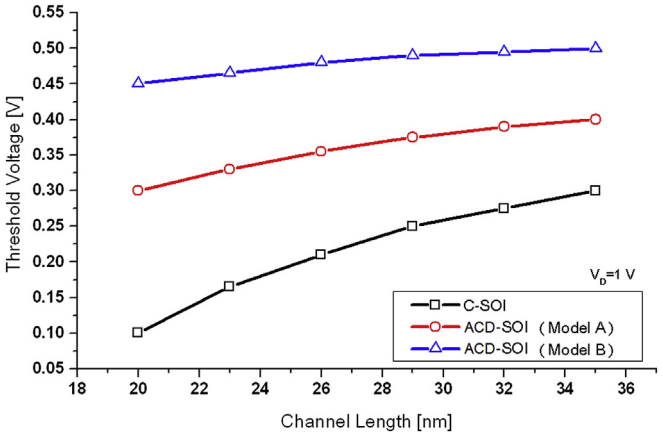

Fig. 13. Threshold voltage of the ACD-SOI and C-SOI structures versus channel length up to 20 nm.

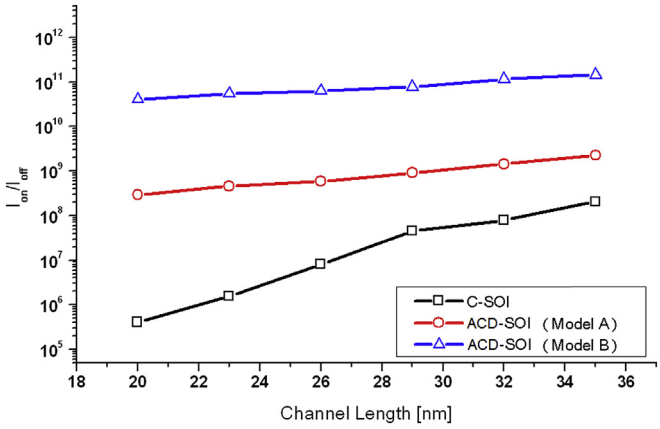

Fig. 14. Ratio of I_{on} and I_{off} (I_{on}/I_{off}) versus channel length up to 20 nm for the ACD-SOI and C-SOI structures.

a function of the doping density distribution slope when it decreases with slope enlargement. The chief reason of the DIBL reduction that is one of the SCEs affairs is employing novel doping distribution in the channel that causes less penetration of source and drain depletion region into the channel and consequent lower interaction of them. So this phenomenon leads to lower DIBL and leakage current in the ACD-SOI structure. Thus a large value of the I_{on}/I_{off} in the ACD-SOI structure is expectable due to the prominent leakage current reduction and I_{on}/I_{off} gets improved by slope increment. Consequently, the final result that we get from the calculated data for various slopes of the vertical graded distribution is higher slope causes better electrical and thermal performance of the fully-depleted SOI-MOSFETs especially for the short channel devices.

5. Conclusion

An amended channel doping (ACD) engineering has been demonstrated excellent performances in term of electrical and thermal applications. By employing vertical graded doping in the channel we achieved hot electron degradation, short channel effects (SCEs), gate induced drain lowering (GIDL), leakage current and self-heating effect (SHE) improvement. Achieving the high potential barrier height helps for SCEs and leakage current suppression because of less injected carriers

Table 1
Maximum lattice temperature and the maximum electron temperature for various doping parameters in the channel.

Structure	Channel doping parameters	Maximum lattice temperature	Maximum electron temperature
C-SOI	$N_H = 1 \times 10^{17}$ cm^{-3} $N_L = 1 \times 10^{17}$ cm^{-3} $S = 0$ cm^{-4}	731 K	4226 K
ACD-SOI (Model A)	$N_H = 2.5 \times 10^{17}$ cm^{-3} $N_L = 7.5 \times 10^{16}$ cm^{-3} $S = 1.75 \times 10^{23}$ cm^{-4}	678 K	4180 K
ACD-SOI (Model B)	$N_H = 5 \times 10^{17}$ cm^{-3} $N_L = 5 \times 10^{16}$ cm^{-3} $S = 4.5 \times 10^{23}$ cm^{-4}	627 K	4135 K
ACD-SOI (Model C)	$N_H = 7.5 \times 10^{17}$ cm^{-3} $N_L = 2.5 \times 10^{16}$ cm^{-3} $S = 7.25 \times 10^{23}$ cm^{-4}	589 K	4095 K
ACD-SOI (Model D)	$N_H = 1 \times 10^{18}$ cm^{-3} $N_L = 1 \times 10^{16}$ cm^{-3} $S = 9.9 \times 10^{23}$ cm^{-4}	557 K	4056 K
ACD-SOI (Model E)	$N_H = 2.5 \times 10^{18}$ cm^{-3} $N_L = 7.5 \times 10^{15}$ cm^{-3} $S = 2.49 \times 10^{24}$ cm^{-4}	523 K	4003 K
ACD-SOI (Model F)	$N_H = 5 \times 10^{18}$ cm^{-3} $N_L = 5 \times 10^{15}$ cm^{-3} $S = 4.99 \times 10^{24}$ cm^{-4}	490 K	3963 K
ACD-SOI (Model G)	$N_H = 7.5 \times 10^{18}$ cm^{-3} $N_L = 2.5 \times 10^{15}$ cm^{-3} $S = 7.49 \times 10^{24}$ cm^{-4}	416 K	3925 K
ACD-SOI (Model I)	$N_H = 1 \times 10^{19}$ cm^{-3} $N_L = 1 \times 10^{15}$ cm^{-3} $S = 9.99 \times 10^{24}$ cm^{-4}	359 K	3893 K

Table 2
Effective electron mobility, DIBL, and I_{on}/I_{off} for various doping parameters in the channel.

Structure	Channel doping parameters	DIBL	I_{on}/I_{off}	Effective electron mobility
C-SOI	$N_H = 1 \times 10^{17}$ cm^{-3} $N_L = 1 \times 10^{17}$ cm^{-3} $S = 0$ cm^{-4}	100 mV/V	2.04×10^{8}	650 cm^2/vs
ACD-SOI (Model A)	$N_H = 2.5 \times 10^{17}$ cm^{-3} $N_L = 7.5 \times 10^{16}$ cm^{-3} $S = 1.75 \times 10^{23}$ cm^{-4}	96 mV/V	3.24×10^{8}	535 cm^2/vs
ACD-SOI (Model B)	$N_H = 5 \times 10^{17}$ cm^{-3} $N_L = 5 \times 10^{16}$ cm^{-3} $S = 4.5 \times 10^{23}$ cm^{-4}	93 mV/V	4.66×10^{8}	530 cm^2/vs
ACD-SOI (Model C)	$N_H = 7.5 \times 10^{17}$ cm^{-3} $N_L = 2.5 \times 10^{16}$ cm^{-3} $S = 7.25 \times 10^{23}$ cm^{-4}	90 mV/V	6.23×10^{8}	528 cm^2/vs
ACD-SOI (Model D)	$N_H = 1 \times 10^{18}$ cm^{-3} $N_L = 1 \times 10^{16}$ cm^{-3} $S = 9.9 \times 10^{23}$ cm^{-4}	86 mV/V	7.94×10^{8}	527 cm^2/vs
ACD -SOI (Model E)	$N_H = 2.5 \times 10^{18}$ cm^{-3} $N_L = 7.5 \times 10^{15}$ cm^{-3} $S = 2.49 \times 10^{24}$ cm^{-4}	83 mV/V	9.98×10^{8}	526 cm^2/vs
ACD-SOI (Model F)	$N_H = 5 \times 10^{18}$ cm^{-3} $N_L = 5 \times 10^{15}$ cm^{-3} $S = 4.99 \times 10^{24}$ cm^{-4}	80 mV/V	2.25×10^{9}	525 cm^2/vs
ACD-SOI (Model G)	$N_H = 7.5 \times 10^{18}$ cm^{-3} $N_L = 2.5 \times 10^{15}$ cm^{-3} $S = 7.49 \times 10^{24}$ cm^{-4}	76 mV/V	1.81×10^{10}	522 cm^2/vs
ACD-SOI (Model I)	$N_H = 1 \times 10^{19}$ cm^{-3} $N_L = 1 \times 10^{15}$ cm^{-3} $S = 9.99 \times 10^{24}$ cm^{-4}	70 mV/V	1.43×10^{11}	518 cm^2/vs

into the channel in weak inversion regime. Furthermore hot electron degradation and GIDL improvement depended on the electric field maximum that reduces in the ACD-SOI structure compared to the conventional fully-depleted SOI MOSFET with uniform doping distribution (C-SOI). Generally, decrement of the electric field peak and maximum value of the electron temperature at drain junction are signs for reliability improvement. SCEs affairs such as DIBL and threshold voltage roll off are suppressed which causes leakage current and power consumption reduction. Thus the large value of on-off current ratio (I_{on}/I_{off}) is achieved according to the prominent decrement of the off current. Furthermore, by employing low doping density in the ACD-SOI structure in comparison with the C-SOI structure near the buried oxide layer, suppression of SHE and less lattice temperature is achieved. We get result that higher slope of the vertical graded doping distribution access better electrical and thermal performances. So, results show that the proposed structure is a good choice as a reliable device for high temperature and low power applications.

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