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MIXED SIGNAL LETTER

A 1.8-V 11-bit 40-MS/s 21-mW pipelined ADC

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Abstract A set of low-power techniques is proposed to realize low power design in pipeline analog-to-digital converter (ADC). These techniques include removing the active S/H (i.e., SHA-less), sharing the opamp between the adjacent multi-bit-per-stages, low-power high-efficiency high-swing amplifier technique. Also, a new sampling topology is proposed to minimize aperture error by matching the time constant between the two input signal paths. All these skills are verified by simulation in the design of the 1.8-V 11-bit 40-MHz ADC in a 0.18-μm CMOS process with power dissipation 21-mW, signal-to-noise-and-distortion ratio (SNDR) 65-dB, effective number of bit (ENOB) 10.5-bit, spurious free dynamic range (SFDR) 78-dB, total harmonic distortion (THD) −75.4-dB, signal-to-noise ratio (SNR) 65.4-dB and figure-of-merit (FOM) 0.18 pJ/step.

Keywords Analog-to-digital converter · Pipeline ADC · High-swing amplifier · Low-power · SHA-less · Pipeline · Opamp-sharing

1 Introduction

Low-power analog-to-digital converters (ADCs) with 10–12-bit resolution and several tens of MHz sampling rates are recognized as one of the significant components in portable or battery-operated commercial applications including data communication and image signal processing systems. Recently, a lot of low-power technologies are proposed and verified in several designs. However, the time-interleaving architecture [1, 2] is easily limited by offset and gain mismatches as well as aperture errors between the interleaved channels. The performance of the pseudo-differential architecture [3] compared with that of the fully differential one, is sensitive to the common mode voltage and substrate or power supply noise. Complex calibration schemes and/or circuit techniques [4–8], which are usually needed to enhance the linearity and/or correct the mismatches such as compensating low gain, low bandwidth and incomplete settling of opamps, need complicated algorithm, additional digital circuitry and extra calibration cycles. SHA-less and opamp-sharing are two important ways for low-power pipelined ADC design [9–13]. However, they also bring some drawbacks affecting the ADC performance, such as nonlinearity and distortion. How to tradeoff and get rid of these bad factors are the hot points in the low-power Pipelined ADC design area. Reference [9] takes use of dummy sampling capacitances and complicated digital calibration without opamp-sharing to enhance the SNR and SFDR performance. Reference [10] is also without opamp-sharing and use traditional simple 1.5b/stage architecture when utilizing SHA-less. the proposed structure in [11] may not be suitable for the ADCs that are expected to run at the maximum achievable sampling rate for a given resolution and technology, Because the opamp used in the proposed first stage needs to be faster, simultaneously meaning more power consumption, than the one in the traditional first stage. The proposed structures in

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[12, 13], taking use of some techniques proposed in [14], need additional clocks of different duty cycle. This paper combines SHA-less, opamp-sharing, multibit-per-stage techniques together into the whole ADC, including the first stage. So only two opamps are used, which makes the 11bit ADC the one using the least opamp in the counterparts up to now, very simple and easy to design for SOC. A new scheme of time constant matching between the two input signal paths and a high-efficiency opamp are proposed, which allow the ADC, even not using digital calibration, to get good SNR and SFDR, and is beneficial for small area and low power consumption.

This paper is organized as follows. Sect. 2 presents the architectural considerations for the ADC; Sect. 3 gives the design and circuit realization of the ADC; Sect. 4 displays experimental results, followed by a conclusion in Sect. 5.

2 ADC architecture

The main power dissipation of the pipeline ADC comes from amplifiers. The power dissipation could be cut down by more than 50 percent by reduction of the number of amplifiers through the amplifier-sharing and SHA-less technology compared with the normal architecture with S/H [15]. The proposed ADC architecture is shown in Fig. 1. There are five stages in the ADC. Each of the first four stages is 2.5-bit per stage and generates 2 effective bits and the last flash ADC gives 3 effective bits. There are only two active opamps utilized in the ADC. The first opamp is shared by the first SHA-less stage and the second stage, and the second opamp is shared by the third and the fourth stages. Each flash ADC in the first four stages consists of 6 low power dynamic comparators and the last flash ADC is built up with 7 comparators. The clock generator, digital correction logic and current-to-voltage bias voltage generation circuit are also included in the ADC.

3 Circuits design of the ADC

3.1 SHA-less and 2.5 bit-per-stage with OPAMP-sharing

The first stage without explicit S/H is 2.5-bit architecture, and shares the opamp with the stage 2. The architecture is shown in Fig. 2(a), which includes MDACs and a 3-bit flash ADCs. The input signal is sampled on cs1, cs2, cs3, cs4 and cc1–6 of the flash ADC by bootstrapped switches with the same clock phase Q3P, which can ensure the time constants of the two paths equal as introduced in next Sect. 3.2. In phase Q4 the sampling capacitance cs1–4 are floated and cc1–6 are charged with reference voltage, the comparators work. When Q4 turn low, the outputs of comparators are latched and 3 bits digital data and control codes are generated. In Q2, the opamp is interchanged into stage 1, and the control codes are selected for MDAC1 to configure and amplify the residue voltage, which is simultaneously sampled by the stage 2. In the phase Q1, the 3 bits digital data and control codes of stage 2 are generated, and the opamp is interchanged into stage 2 to generate residue voltage for the next stage. The clock generation scheme is given in Fig. 2(b). The input CK signal, which is twice the frequency of the ADC actual operation clock, is divided through a DFF by 2 to generate non-overlap clocks Q1 and Q2 with duty cycle nearly 0.5. The Q3 and Q4, with duty cycle 0.25, are generated from the combination of CK and Q1.

The comparator in the 3-bit flash ADC is shown in Fig. 3. The sampling route of the comparator is similar to that of the MDAC1. According to the charge conversation at the bottom plate of Cs1 and Cs2, the reference voltage for the comparator can be got from the ratio of Cs1 to Cs2 with the equation as described in Fig. 3.

3.2 A new scheme of time constant matching between the two input signal paths

There will be the aperture error defined as V_e if the MDAC1 and the 3 bit flash ADC1 of stage 1 do not match well [14].

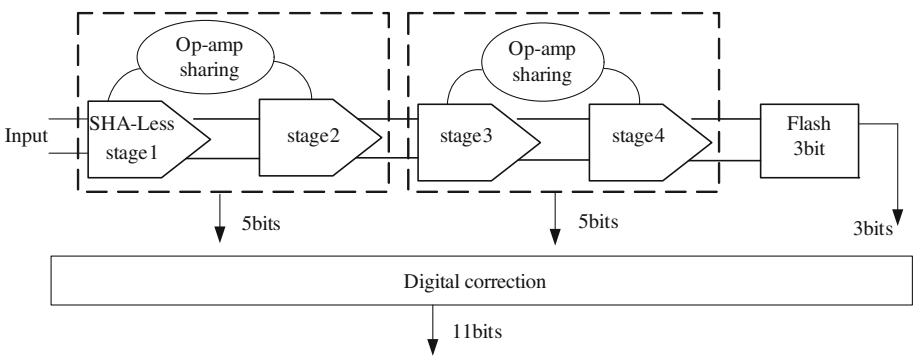

Fig. 1 The ADC architecture

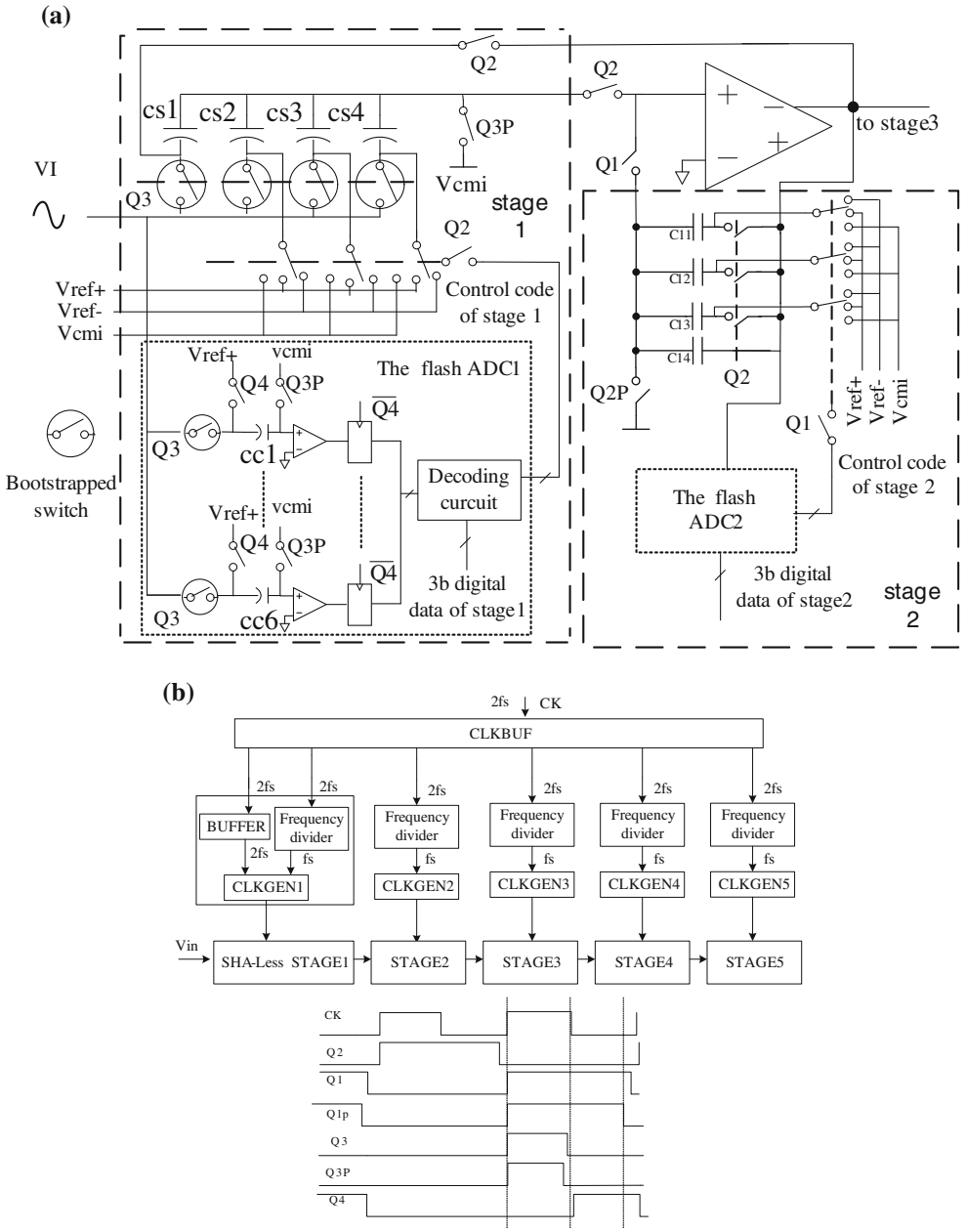

Fig. 2 **a** The architecture of the stage 1 and stage 2 without explicit S/H; **b** The clock generation scheme and clock diagram

For the flash ADC1 of the 2.5-bit first stage, the error voltage range allowed for the digital redundancy is less than 1/8*Vref*. If the bandwidth of the input sampling network is much larger than that of the input signal (assuming $f_{in} \leq 0.1 \cdot (1/\tau)$) then the ADC can generate correct digital output words even with a 20% time constant mismatch

$$\Delta \leq \frac{1}{8 \cdot 2\pi \cdot f_{in} \cdot \tau} = \frac{1}{8 \cdot 2\pi \times 0.1} \approx 0.2 \tag{1}$$

So even in the presence of high-frequency signals at the input, it is possible to obtain good dynamic performance by matching the sampling networks for the MDAC1 and the comparators of the flash ADC1 in terms of topology and time constants.

Here, The MDAC1 and the flash ADC1 have their own input sampling switches shown in Fig. 2(a). In order to keep the time constant τs ($\tau = RC$) of the signal paths equal, the input sampling switches of the flash ADC1 and MDAC1 are both bootstrapped, and the sizes of these switches are chosen proportionally. The "on" resistance of the bootstrapped switch R_{on} is given by (2),

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{W}{L}(V_{DD} - V_{TH})} \tag{2}$$

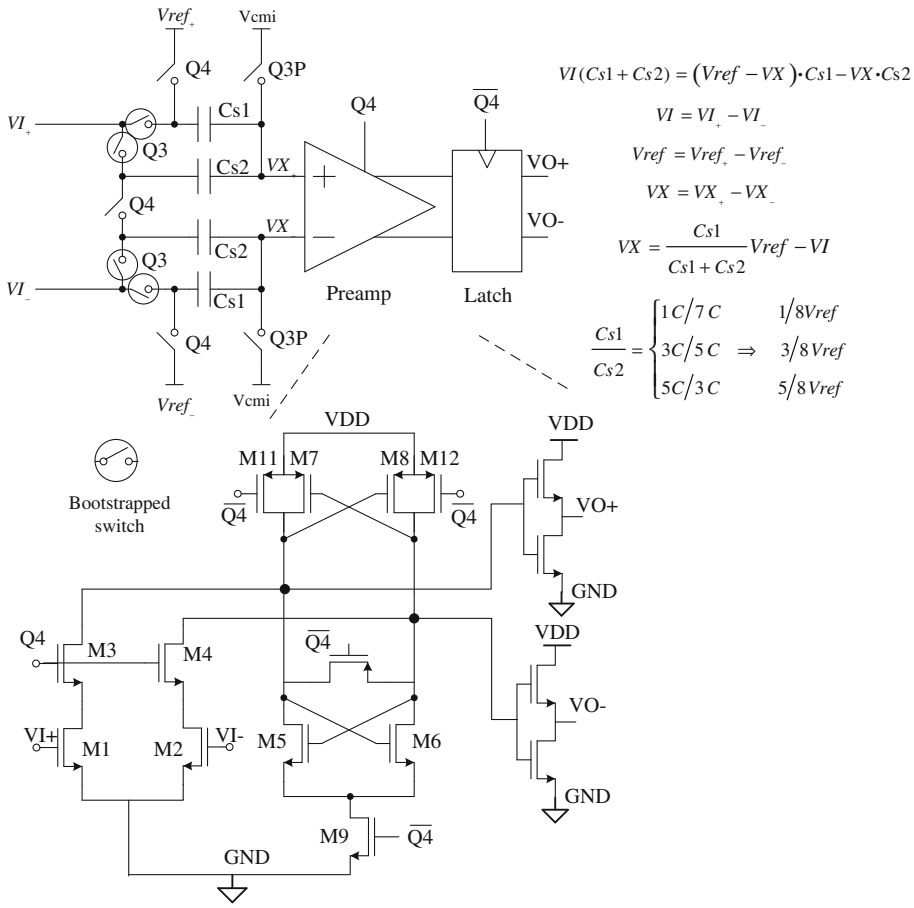

Fig. 3 The comparator used in the flash ADC

From the above formula, there is

$$\frac{W}{L} \propto \frac{1}{R_{on}} \tag{3}$$

To keep the time constant τs equal, there must be:

$$\frac{R_{SM}}{R_{SF}} = \frac{C_{SF}}{C_{SM}} \tag{4}$$

So the sizes of input bootstrapped sampling switches are given by the ratio as follow:

$$\frac{\left(\frac{W}{L}\right)_{SM}}{\left(\frac{W}{L}\right)_{SF}} = \frac{C_{SM}}{C_{SF}} \tag{5}$$

R_{SM}, C_{SM} represent the equivalent switch resistance and capacitance, respectively, in each identical signal path of the MDAC1.R_{SF}, C_{SF} mean the equivalent switch resistance and capacitance in each identical signal path of the flash ADC1. $\left(\frac{W}{L}\right)_{SM}$, $\left(\frac{W}{L}\right)_{SF}$ represent the sizes of the bootstrapped switches of the MDAC1 and the flash ADC1, respectively.

With symmetrical architecture and meticulous layout, the signal transmission time constant mismatch Δ·τ can be designed to be very small so that the error voltage including comparator offset is only 60-mV, much smaller than 1/8*Vref*, 200-mV, and can be corrected by digital redundancy.

3.3 The proposed low-power high-swing OPAMP

Normally, under 1.8 v supply, three kinds of opamp topology are feasible for high speed high resolution pipeline ADC: two stages, folded cascode and single-stage telescopic. The two stages opamp needs compensation and more than twice the power consumption of single stage architecture. The folded cascode opamp also consume more power than a single-stage telescopic architecture which has good merits on power efficiency and large bandwidth while the output swing is small. If the output swing can be enlarged to a considerable level, the telescopic architecture will be the best choice for the low power pipeline ADC. To solve the contradictory problem of the high swing and low power, some techniques have been adopted in the chosen telescopic opamp in this paper in the Fig. 4. Firstly, the top two load transistors M7, M8 and the tail transistor M0 in dashed are deliberately driven deep into the linear region. It is important to improve differential swing as the tail transistor cuts into the output swing from both sides of the amplifier. Also, the

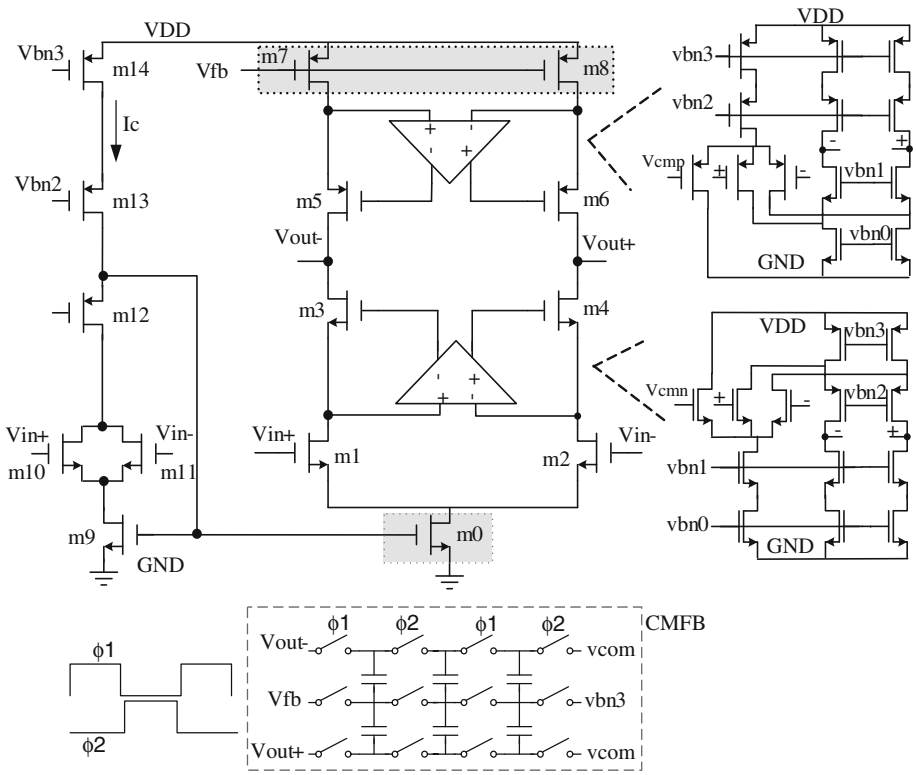

Fig. 4 The architecture of the proposed opamp

Table 1 The performance of the proposed opamp

Parameters	Performance
Process (μm)	TSMC 0.18
Power supply voltage (V)	1.8
DC gain (dB)	99
Input common voltage (V)	0.7
Output common voltage (V)	0.9
Phase margin (deg)	62
Output swing peak-to-peak (V)	2
Unity gain bandwidth (MHz)	880
Power consumption (mW)	8.95

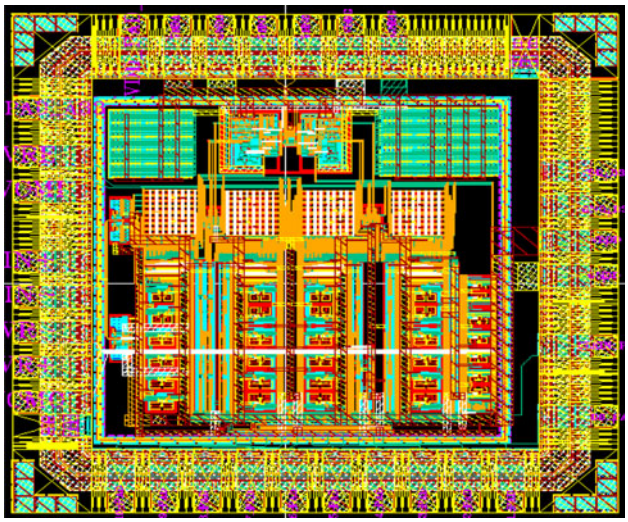

Fig. 5 The layout of the proposed ADC

elimination of voltage margin across the tail and the load devices itself contributes to a swing enhancement of 4 voltage margins. This benefit of increased swing by pushing the load and tail transistors in the linear region, however, is accompanied by degraded common-mode rejection ratio (CMRR), PSRR, and differential gain of the amplifier [16]. Additionally, as in the case of the no-tail telescopic amplifier, performance parameters of the amplifier are sensitive to the input common-mode voltage level. The reduction in dc gain has been compensated for by a regulated cascode gain enhancement scheme, which is the second technique. The third technique, for improving CMRR and PSRR, is that the bias voltage at the gate of M0 can be adaptively adjusted by a replica circuit consisting of M9–M14, in which M10, M11 will sense the input common-mode voltage of the core differential pair of M1 and M2. If the common-mode voltage is going down, the M9 will go into triode region. However, to keep the same dc current Ic from M13 and M14, its gate voltage will be pulled up by the negative feedback replica bias. The basic goal of the replica tail feedback is to keep the tail current constant despite variations in the input common-mode voltage level. So, the M0 could be biased at triode region by this way with a large output resistance, which will

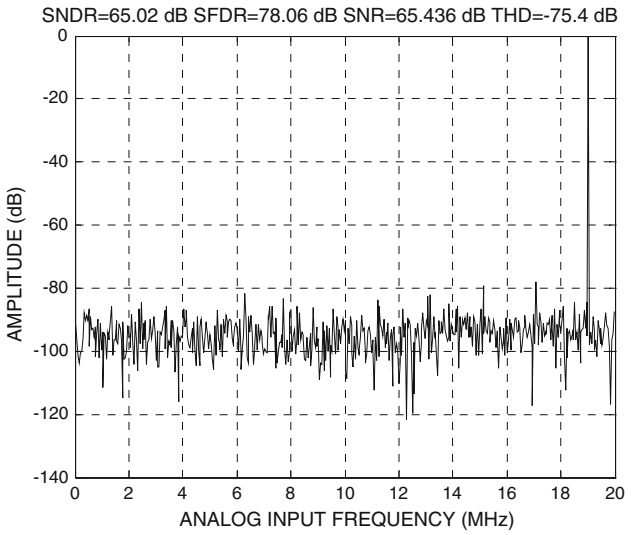

Fig. 6 The FFT performance of the proposed ADC with 19-MHz full-swing input signal

contribute about 0.2 v dynamic swing; the small-signal analysis shows that the effective resistance looking into the tail-current transistor M0 can be approximately represented by

$$R_{tail} = \mathrm{r}_{M0}(1 + g_{m9} \cdot r_{m9} \cdot g_{m10} \cdot r_{m10} \cdot g_{m12} \cdot r_{m12}) \quad (6)$$

And the CMRR is given as follows:

$$CMRR = (1 + 2g_{m1,2}R_{tail})g_{m7,8}(r_{o1,2} \cdot g_{m3,4}r_{m3,4} \parallel r_{o7,8} \cdot g_{m5,6}r_{m5,6}) \quad (7)$$

A high CMRR can be got by large R_{tail}, which is easily fulfilled through utilizing long channel transistor M9, M10, M11, M12.Typically, about 50–60 dB enhancement of CMRR will be achieved. The cascade transistors of M3, M4, M5 and M6 will be biased in moderate inversion, and has the largest transconductance (g_m) performance under a certain bias current. Its saturation voltage is kept around 100 mV. An SC common-mode feedback circuit is applied to keep the output common voltage at half of the supply. The performance of the opamp is given in Table 1. The output peak-to-peak swing of the opamp can reach 2-V, and actually for linearity consideration, the *Vref* range is defined to be 1.6-V.

4 Implementation and results

In a TSMC 0.18-μm CMOS 1P6 M process, the whole ADC is designed and simulated with Hspice in all process corners with good performance. The layout of the ADC is shown in Fig. 5. It occupies an area of 1.4 mm × 1.5 mm. The total power consumption is 21-mW at 1.8-V and 40-MHz sampling frequency. The back-end simulation

Table 2 The performance of the ADC in different process corners

Different corners (°C)	SFDR (dB)	SNDR (dB)	THD (dB)	Power dissipation (mW)
TT 75	75.4	64.4	−73.2	21
SS 75	78	65	−75.4	21
FF 75	73.3	63.2	−71.1	21

results of the data extracting from layout in Fig. 6 shows that SNDR, SNR, SFDR THD are 65, 65.4, 78, −75.4 dB, respectively. The THD is calculated from 2nd through 5th order harmonics. Table 2 gives the performance results under different corners with 19-MHz full-swing input signal. The figure-of-merit (FOM) of this ADC is 0.18 pJ/step.

5 Conclusion

Several feasible low-power techniques, including removing the active S/H (SHA-less) with a new sampling topology, sharing the opamp between the adjacent multi-bit-per-stages, low-power high-efficiency high-swing amplifier technique, are proposed and verified successfully through the design of the proposed 1.8-V 11-bit 40-MS/s 21-mW pipelined ADC in TSMC 0.18 mixed-signal CMOS process with very competitive performance. The FOM is 0.18 pJ/step, which makes the proposed ADC among the most efficient ADCs.

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