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A Novel Reversible BCD Adder For Nanotechnology Based Systems

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Abstract: This paper proposes two reversible logic gates, HNFG and HNG. The first gate HNFG can be used as two Feynman Gates. It is suitable for a single copy of two bits with no garbage outputs. It can be used as "Copying Circuit" to increase fan-out because fan-out is not allowed in reversible circuits. The second gate HNG can implement all Boolean functions. It also can be used to design optimized adder architectures. This paper also proposes a novel reversible full adder. One of the prominent functionalities of the proposed HNG gate is that it can work singly as a reversible full adder unit. The proposed reversible full adder contains only one gate. We show that its hardware complexity is less than the existing reversible full adders. The proposed full adder is then applied to the design of a reversible 4-bit parallel adder. A reversible Binary Coded Decimal (BCD) adder circuit is also proposed. The proposed circuit can add two 4-bit binary variables and it transforms the result into the appropriate BCD number using efficient error correction modules. We show that the proposed reversible BCD adder has lower hardware complexity and it is much better and optimized in terms of number of reversible gates and garbage outputs with compared to the existing counterparts.

Keywords: Reversible Logic, Quantum Computing, Reversible Gate, Full Adder, BCD Adder

INTRODUCTION

Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where $K=1.3806505*10^{-23}m^2kgs^{-2}K^{-1}$ (joule/kelvin) is the Boltzmann's constant and T is the temperature at which operation is performed[1,5]. In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs[2,3].

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. Thus, reversible logic circuits offer an alternative that allows computation with arbitrarily small energy dissipation. Furthermore, reversible circuits are of major interest in optical computing, low power design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic. Reversible computation in a system can be performed if the system is composed of reversible gates[4].

A circuit (gate) is reversible if there is a one-to-one correspondence between the inputs and the outputs. Thus, any reversible gate has the same number of input and output lines, and it implements a permutation from input values to output values. Neither feedback nor fan-out is allowed in reversible logic[5,6]. Consequently, synthesis of reversible logic is different from irreversible logic synthesis. One of the major constraints in reversible logic is to minimize the number of reversible gates used and garbage outputs produced. Garbage output refers to the output that is not used for further computations[8].

A logic synthesis technique using reversible gate should have the following features[7]:

1. Use minimum number of garbage outputs
2. Use minimum input constants
3. Keep the length of cascading gates minimum
4. Use minimum number of gates

In this research, two new reversible logic gates are introduced. A novel reversible full adder is also presented. It is then compared with the existing reversible full adders. Furthermore, this paper introduces a novel reversible BCD adder using the proposed HNG gate with minimal number of reversible gates and garbage outputs.

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MATERIALS AND METHODS

Reversible Logic Gates: There is a number of existing reversible logic gates such as Feynman Gate, FG[10], Toffoli Gate, TG[11], Fredkin Gate, FRG[12], New Gate, NG[13], and New Toffoli Gate, NTG[15,16].

A 2*2 Feynman Gate, also known as controlled NOT (1-CNOT), depicted in Fig. 1. It implements the logic functions: P=B, and Q=A⊕B. Feynman Gate is the most suitable gate for a single copy of a bit. A '0' in the second input will copy the first input in both outputs of the gate (Fig. 2). Thus, Feynman Gate is the most suitable gate for single copy of bit since it is not producing any garbage output[14].

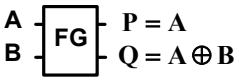

Fig. 1: Feynman Gate.

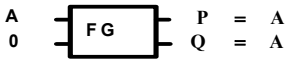

Fig. 2: Feynman Gate as copying output

A generalized, k-way, Toffoli Gate has k + 1 inputs: k control inputs, that are copied to the first k outputs, and one other input that is complemented if all control inputs are 1s and is directly copied to the last output otherwise[5]. A 3-input, 3-output Toffoli Gate is shown in Fig. 3. The inputs 'A' and 'B' are passed as first and second output respectively. The third output is controlled by 'A' and 'B' to invert 'C'.

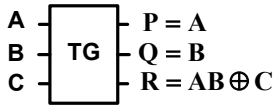

Fig. 3: Toffoli Gate

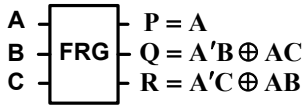

Fig. 4: Fredkin Gate

A 3*3 Fredkin Gate is shown in the Fig 4. Here the input 'A' is passed as first output. Inputs 'B' and 'C' are swapped to get the second and third output which is controlled by input 'A'. If A=0, then the outputs are simply duplicates of the inputs; otherwise if A= 1, then the two input lines (B and C) are swapped.

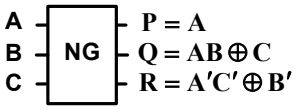

Fig. 5: New Gate

A 3*3 New Gate (NG) depicted in Fig. 5. It can be defined as I_v=(A, B, C) and O_v=(P=A, Q=AB⊕C, R=A′C′⊕B′). Where I_v and O_v are the input and output vectors respectively.

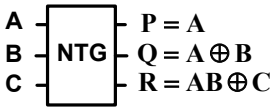

Fig. 6: New Toffoli Gate

A 3*3 New Toffoli Gate (NTG) also known as Peres Gate (PG), is equivalent to the transformation produced by a Toffoli Gate followed by a Feynman Gate. Fig. 6 shows the block diagram of 3*3 New Toffoli Gate (NTG). Several other types of reversible gates have also been used.

New 4*4 Reversible Gates: This paper proposes two new reversible logic gates: HNFG and HNG. Gates HNFG and HNG are shown in Fig. 7 and Fig. 8 respectively; the corresponding truth tables of the gates are shown in the table 1. and table 2 respectively. It can be verified from the truth tables that the input pattern corresponding to a particular output pattern can be uniquely determined.

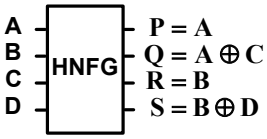

Fig. 7: Proposed reversible HNFG gate

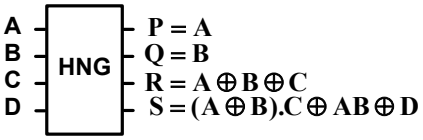

Fig. 8: Proposed reversible HNG gate

Gate width of HNFG and HNG is 4. In the other words, HNFG and HNG are 4-input, 4-output reversible gates. Furthermore, both of them are two-through gates, which means that two input variables are also outputs.

Each HNFG gate can be used as two well-known 2*2 Feynman gates. It also can be used as "Copying Circuit" to increase fan-out because fan-out is not allowed in reversible circuits. It is suitable for a single copy of two bits with no garbage outputs as depicted in Fig. 9.

Table 1: Truth table of the proposed reversible HNFG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	0	0	1	1
0	1	0	1	0	0	1	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	0	0
1	0	1	1	1	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Table 2: Truth table of the proposed reversible HNG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

HNG gate can be used for implementing arbitrary functions. HNG gate can implement all boolean functions. The OR and the EX-NOR functions can be simultaneously implemented on HNG (Fig. 10a). The EX-OR function and the NAND function can be implemented as depicted in Fig. 10b. The NOR function can be obtained as shown in Fig. 10c. The AND function can be implemented as depicted in Fig. 10d. The implementation of the HNG gate as NOT function is shown in Fig. 10e.

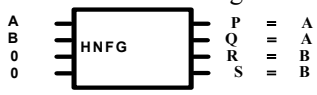

Fig. 9: HNFG gate is suitable for a single copy of two bits

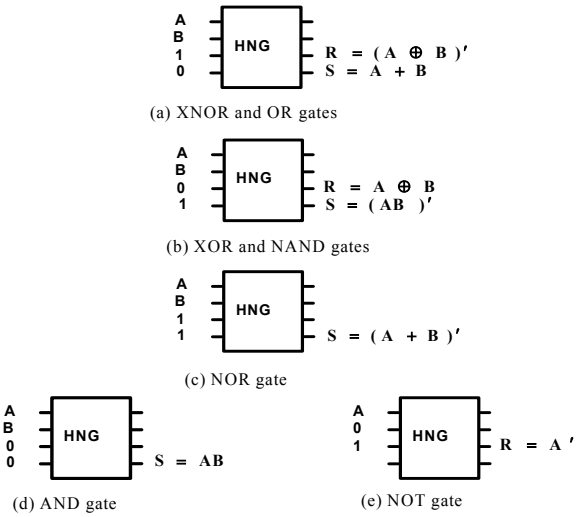

Fig. 10: Proposed HNG gate can implement all boolean functions

New Reversible Full Adder: Full adder circuit is a versatile and widely used element in digital arithmetic processing. Several researchers have proposed reversible full adder circuits[13,19,20,16,18,8,5]. One of the prominent functionalities of the HNG gate is that it can work singly as a reversible full adder unit. The implementation of the proposed HNG gate as the reversible full adder is depicted in Fig. 11.

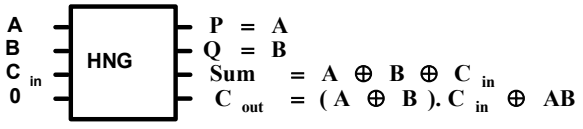

Fig. 11: Proposed HNG gate as Reversible Full Adder

Synthesis of Reversible Circuits: Synthesizing a circuit with reversible gates is different from synthesizing an irreversible circuit. The main differences are the following:

- The number of inputs and outputs are equal.

- We should try to produce minimum number of garbage outputs.
- Neither feedback nor fan-out is allowed in reversible logic; every output can be used only once.

Consequently, in the proposed circuits the constraints are carefully abided.

New Reversible BCD Adder: A BCD adder circuit adds two BCD numbers and converts the result into its equivalent BCD number. The conversion is needed because of the occurrence of overflow of the addition. We use the proposed reversible full adder depicted in Fig. 11 to construct a reversible 4-bit parallel adder shown in Fig. 12.

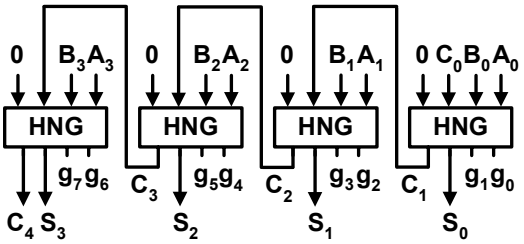

Fig. 12: Proposed reversible 4-bit parallel adder

The proposed reversible BCD adder using proposed HNG and HNFG gates is depicted in Fig. 13. The proposed BCD adder has two reversible 4-bit parallel adders, which require total eight HNG gates. Furthermore, two New Gates and one Toffoli Gate are required in the proposed reversible BCD adder. Two Feynman Gates and one HNFG gate are required to avoid fan-out of bits. As a result, the total number of gates required to construct the reversible BCD adder is 2*4+2+1+2+1=14.

In the proposed BCD adder circuit, we used four proposed reversible full adder circuits to construct a reversible 4-bit parallel adder, and each full adder circuit produces two garbage outputs. So, the total number of garbage outputs generated from the 4-bits reversible adder is eight. The two New Gates and one Toffoli Gate produce six garbage outputs. The two Feynman Gates and one HNFG gate, which are used for copying bits, do not produce any garbage outputs. As a result, the total number of produced garbage outputs is 2*8+6=22.

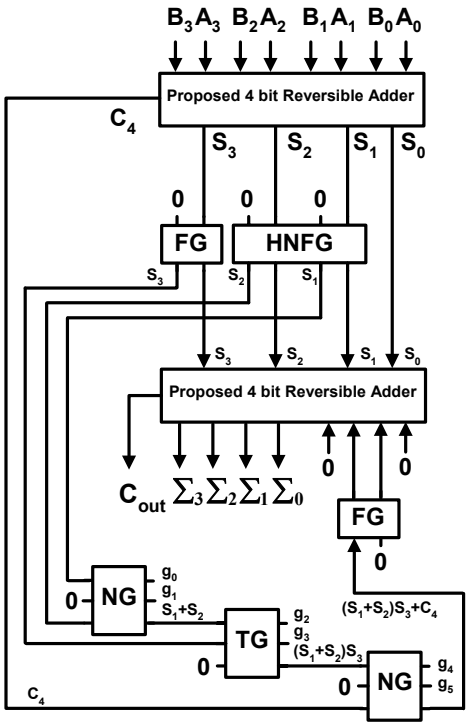

Fig. 13: Proposed reversible BCD adder

RESULTS AND DISCUSSION

Evaluation of The Proposed Reversible Full Adder: Our proposed circuit performs better than the existing reversible full adders. An experimental result will comprehend it clearly. Table 3 compares the proposed reversible full adder circuit with the existing counterparts.

One of the major constraints in reversible logic is to minimize the number of reversible gates used. In our full adder design approach we used only one reversible logic gate, so we can state that the proposed circuit is optimal in terms of number of reversible logic gates.

Another significant criterion in designing a reversible full adder is to lessen number of garbage outputs. Every output of the gate that is not used as a primary output or as input to other gate is called garbage output. A heavy price is paid for every garbage bit. It has been proved that a reversible full-adder circuit requires at least two garbage outputs to make the output combinations unique, which is the primary condition for a reversible circuit[17]. The proposed reversible full adder circuit produces two garbage

outputs, so it is optimal in terms of number of garbage outputs.

Table 3: Comparative experimental Result of different reversible full adder circuits

	No. of Gates	No. of Garbage Outputs	Hardware Complexity	
			Total Clock Cycle	Total Logical Calculation
This Work	1	2	1σ	5α+2β
Existing Circuit[5]	2	2	2σ	4α+2β
Existing Circuit[8]	1	2	1σ	6α+3β+3δ
Existing Circuit[16]	2	2	2σ	4α+3β+3δ
Existing Circuit[17,18]	3	2	3σ	4α+3β+3δ
Existing Circuit[13]	3	3	3σ	5α+4β+6δ
Existing Circuit[19]	5	5	5σ	10α+20β+10δ
Existing Circuit[6,20]	4	2	4σ	4α+2β

σ = Unit Clock Cycle
α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation

This work requires only one clock cycle, so we can state that it is optimal in terms of required clock cycles, which is one of the main factors of a circuit.

Only one of the existing circuits[8] has all these optimal properties similar to our proposed full adder circuit (See Table 3). Our proposed circuit is better than [8] in terms of complexity.

Let
α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation
T= Total logical calculation
So, for [8]: T=6α+3β+3δ
For our proposed full adder circuit: T=5α+2β

Thus, the propounded reversible full adder requires less logical calculations than [8], keeping other properties constant. So, Our proposed circuit is better than the full adder circuit presented in [8].

The design in [16] requires two reversible gates (one 3*3 New Gate and one 3 *3 New Toffoli Gate) and produces two garbage outputs. It requires two clock cycles and its total logical calculation is T=4α+3β+3δ. The reversible full adder circuit in [18] requires three reversible gates (one 3*3 New Gate, one 3*3 Toffoli Gate and one 2*2 Feynman Gate) and produces two garbage outputs. It requires three clock cycles and its total logical calculation is T=4α+3β+3δ. The reversible full adder circuit in [13] requires three reversible gates (two 3*3 New Gate and one 2*2 Feynman Gate) and produces three garbage outputs. It requires three clock cycles and its total logical calculation is T=5α+4β+6δ. The design in [19] requires five reversible Fredkin Gate and produces five garbage outputs. It requires five clock cycles and its total logical calculation is T=10α+20β+10δ. The proposed full adder using HNG in Fig. 11 requires only one reversible gate (one HNG gate) and produces only two garbage outputs. It requires 1 clock cycles and its total logical calculation is T=4α+2β. Thus, the proposed full adder design is better than the previous full adder designs of [16,18,13,19].

On the other hand, the proposed full adder circuit requires less gate and clock cycle than [5] and [20], though it requires just one more logical calculation. The extra calculation is just a two input EX-OR gate calculation. The full adder circuits presented in [5] and [20] are not optimal in terms of number of gates and required clock cycles, but our proposed full adder is optimal. Hence, the new reversible full adder design using HNG gate is also better than the existing designs of [5] and [20] and it has the desirable properties.

Evaluation of The Proposed Reversible BCD Adder: The New reversible BCD adder circuit design performs better than the existing reversible BCD adders. An experimental result will comprehend it clearly. Table 4 compares the proposed reversible BCD adder with the existing circuits. It is to be notified that in table 4 we assumed fan-out is not permitted to make a fair comparison.

The proposed BCD adder architecture in Fig.13 uses only 14 reversible gates and produces 22 garbage outputs, compared to 23 reversible gates and 22 garbage outputs implementation of [14]. Thus, our proposed reversible BCD adder is better than [14] in terms of number of gates used. Furthermore, Total Logical Calculation of Our proposed circuit is T=49α+21β+6δ, compared to T=42α+30β+33δ implementation of [14]. Thus, the propounded reversible BCD adder circuit requires less logical calculations than [14].

Table 4: Comparative Analysis of different reversible BCD Adders

	No. of Gates	No. of Garbage Outputs	Total Logical Calculation
This Work	11+2FG+ 1HNFG=14	22	49α+21β+6δ
Existing BCD adder[14]	19+4FG=23	22	42α+30β+33δ
Existing conventional BCD adder plus fanout[9]	11+5FG=16	22	59α+30β+33δ
Existing carry skip BCD adder plus fanout[9]	15+7FG=22	27	75α+48β+36δ

σ = Unit Clock Cycle
α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation

On the other hand, the conventional BCD adder presented in [9] requires 11 reversible gates plus five reversible Feynman Gates as 'Copying Circuits'. The five Feynman Gates are added to the conventional BCD adder presented in [9] because of the fan-out avoidance in reversible circuits. Thus, our proposed circuit requires 14 reversible gates, compared to 16 reversible gates implementation of the conventional BCD adder presented in [9]. Furthermore, Total Logical Calculation of Our proposed circuit is T=49α+21β+6δ, compared to T=59α+30β+33δ implementation of the conventional BCD adder presented in [9]. Thus, we can state that our propounded reversible BCD adder circuit is much better than [9]. If we don't count 'Copying Circuits' in both designs, we see that the proposed circuit is still better than the conventional BCD adder presented in [9] in terms of complexity while both of them requires 11 reversible gates. In this condition, we see that Total Logical Calculation of Our proposed circuit is T=45α+21β+6δ, compared to T=54α+30β+33δ implementation of the conventional BCD adder presented in [9].

The proposed reversible BCD adder is also much better than the existing reversible carry skip BCD adder presented in [9] in terms of number of reversible gates and garbage outputs. The proposed circuit is also much better than the reversible carry skip BCD adder presented in [9] in terms of hardware complexity (See table 4). So, we can state that the proposed reversible BCD adder circuit is better than the existing counterparts.

CONCLUSION

In this paper, we proposed two novel 4*4 reversible logic gates called HNG and HNFG. We have designed a new reversible full-adder circuit that requires only one reversible HNG gate and produces two garbage outputs. Table 3 illustrates that the proposed reversible full adder is better than the previous reversible full adders. We applied the new reversible full adder to the design of a 4-bits reversible full adder. A reversible Binary Coded Decimal (BCD) adder circuit is also proposed. The proposed reversible BCD adder circuit using HNG and HNFG gates can be used for designing large reversible systems, which is the necessary requirement of quantum computers, because quantum computers must be built from reversible components. The proposed BCD adder poses all the good features of reversible logic synthesis. Furthermore, the restrictions of reversible circuits were highly avoided. Table 4 illustrates that the proposed reversible BCD adder is better than the existing counterparts.

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