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A Novel Fault Tolerant Reversible Gate For Nanotechnology Based Systems

[1]Majid Haghparast and [2]Keivan Navi
[1]Islamic Azad University, Science and Research Branch, Tehran, Iran
[2]Faculty of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran

Abstract: This paper proposes a novel reversible logic gate, NFT. It is a parity preserving reversible logic gate, that is, the parity of the outputs matches that of the inputs. We demonstrate that the NFT gate can implement all Boolean functions. It renders a wide class of circuit faults readily detectable at the circuit's outputs. The proposed parity preserving reversible gate, allows any fault that affects no more than a single signal to be detectable at the circuit's primary outputs. The NFT gate can be used to make fault tolerant reversible logic circuits. We demonstrate how the well-known, and very useful, Toffoli gate can be synthesized from only two parity-preserving reversible gates. We show that our proposed parity-preserving Toffoli gate is much better in terms of number of reversible gates, number of garbage outputs and hardware complexity with compared to the existing counterpart.

Keywords: Quantum computing, Reversible logic gate, Fault tolerant, Boolean functions, Toffoli gate

INTRODUCTION

Traditional irreversible hardware computation inevitably leads to energy dissipation. This is due to the fact that the loss of each one bit of information dissipates an amount of KTln2 joules of energy, where $K=1.3806505*10^{-23}JK^{-1}$ is the Boltzmann's constant and T is the absolute temperature at which computation is performed[1]. The amount of energy dissipation in a system increases in direct proportion to the number of bits that are erased during computation[2]. Bennett showed that to avoid KTln2 energy dissipation in a logic circuit, the circuit must be built with reversible logic gates[3]. This proves that reversible logic is a promising area of study with regard to the further technological advances. A gate (circuit) is reversible if it maps each input assignment to a unique output assignment, that is, if the mapping of inputs to outputs is bijective. Thus, the number of inputs and outputs in a reversible gate or circuit are equal. Such gates (circuits) allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs[4,5,6]. Reversible logic has received significant attention in recent years. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, quantum computing and nanotechnology based systems. Two major problems with reversible logic synthesis are[2,5,6]:

1- Fan-out is not allowed
2- Feedback (Loop) is not allowed

Thus, the synthesis of reversible logic circuit is significantly more complex than the conventional logic synthesis[8]. It is also more difficult to make a fault-tolerant reversible circuit than a conventional logic circuit.

In this paper, a parity-preserving reversible logic gate is presented. It can be used to make fault tolerant reversible logic circuits. It is applied to the design of a parity-preserving Toffoli gate. We demonstrate that the proposed parity-preserving Toffoli gate is better than the existing counterpart.

MATERIALS AND METHODS

Basic Concepts: Several reversible logic gates have been proposed. Among them are Feynman Gate, FG[7], Toffoli Gate, TG[8], Fredkin Gate, FRG[9], New Gate, NG[10] and Feynman Double Gate, F2G[11]. Commonly used reversible logic gates are depicted in Fig. 1 respectively.

Definition 1: Garbage output refers to the output that is not used for further computations[14].

Definition 2: If a reversible gate has k inputs, and therefore k outputs, we call it a reversible k*k gate.

Definition 3: Let $I_v=(A, B, C)$ and $O_v=(P=A, Q= A\oplus B, R= A\oplus C)$ be the input and output vector of a 3*3

Corresponding Author: Majid Haghparast, Islamic Azad University, Science and Research Branch, Tehran, Iran.

Feynman Double Gate, (F2G). The F2G gate is a Feynman Gate with an extra input and one more output, which along with the control input 'A' define a second controlled NOT operation[11]. A 3*3 Feynman Double Gate is depicted in Fig. 1e respectively. For more information about reversible gates see[15].

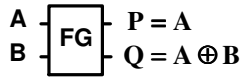


Fig. 1a: Feynman Gate.

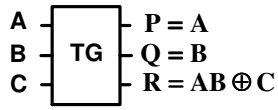


Fig. 1b: Toffoli Gate.

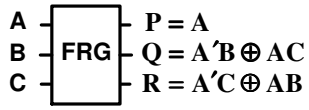


Fig. 1c: Fredkin Gate.

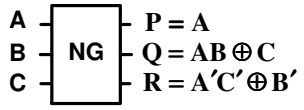


Fig. 1d: New Gate.

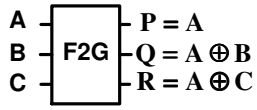


Fig. 1e: Feynman Double Gate.

Fig. 1: Commonly used reversible logic gates

Parity Preserving Reversible Logic Gates: One of the most widely used methods for error detection in digital logic systems is parity checking. It is because most of arithmetic functions do not preserve the parity of the input data. If the parity of the input data persists throughout the computation, no intermediate checking would be required[11]. There are some problems using standard methods of error detection in reversible circuits, because fan-out is not allowed, and it may increase the number of gates used and the number of garbage outputs produced. Given that reversible logic gates have the equal number of inputs and outputs, a sufficient requirement for parity preservation of a reversible circuit is that each gate be parity-preserving[11]. Thus, we need parity-preserving reversible logic gates to construct parity-preserving reversible circuits. A few parity-preserving reversible logic gates have been proposed. It is to be noted that among the gates depicted in Fig.1, only the gates F2G and FRG are parity-preserving reversible gates. Both of them are one-through gates, which means that one of the input variables is also output. The corresponding truth tables of the gates F2G and FRG are depicted in the tables 1 and 2. It can be verified from the truth tables 1 and 2 that the input pattern corresponding to a particular output pattern can be uniquely determined. The gates F2G and FRG are parity-preserving reversible logic gates because they satisfy the equation A⊕B⊕C=P⊕Q⊕R.

Table 1: Truth table of the paity preserving F2G gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Table 2:Truth table of the paity preserving Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

New Parity Preserving Reversible Gate: Are there other parity-preserving, reversible 3-input, 3-output gates? The answer is affirmative, as evidenced by the gate shown in Fig. 2 respectively. We call the proposed gate depicted in Fig. 2 the "New Fault Tolerant" gate or "NFT". NFT gate can be defined as I_v=(A, B, C) and O_v=(P=A⊕B, Q=B′C⊕AC′, R=BC⊕AC′), Where I_v and O_v are the input and output vectors respectively. The corresponding truth table of the NFT gate is shown in the table 3 respectively. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed reversible NFT gate is parity preserving.

This is readily verified by comparing the input parity A⊕B⊕C to the output parity P⊕Q⊕R. In the other words, the gate NFT satisfies the relation A⊕B⊕C=P⊕Q⊕R.

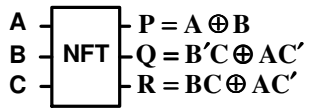


Fig. 2: New parity-preserving reversible gate, satisfying A⊕B⊕C=P⊕Q⊕R.

Table 3: Truth table of the proposed reversible NFT gate

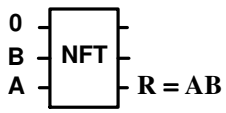
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

NFT gate can be used for implementing arbitrary functions. It can implement all Boolean functions. The implementation of NFT gate as AND function is shown in Fig. 3a. The EX-OR function can be obtained as shown in Fig. 3b respectively. The NOT and the NAND functions can be simultaneously implemented on NFT gate (Fig. 3c). The OR function can be implemented as depicted in Fig. 3d. The EX-NOR function can be obtained by cascading two NFT gates as depicted in Fig. 3e. The NOR function also can be obtained by cascading two NFT gates as depicted in Fig. 3f.

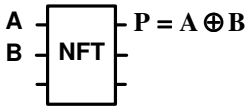
New Design of Parity Preserving TG Circuit: We next show how the functionality of the well-known and very useful Toffoli gate can be synthesized by using only two parity preserving reversible gates.

A parity preserving reversible TG circuit is presented in [11], which is shown in Fig. 4. The circuit requires three reversible gates (one Fredking gate and two F2G gates) and produces two garbage outputs.

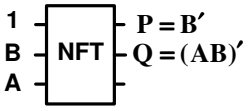
Our proposed design is depicted in Fig. 5 respectively. The circuit shows how one NFT gate and one F2G gate can be used to synthesize a parity-preserving Toffoli gate. It produces one garbage output.



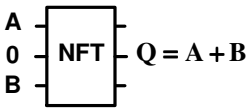
(a) AND gate.



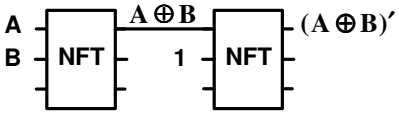
(b) XOR gate.



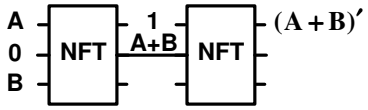
(c) NOT and NAND gates.



(d) OR gate.



(e) XNOR gate.



(f) NOR gate.

Fig. 3: Proposed NFT gate can implement all Boolean functions

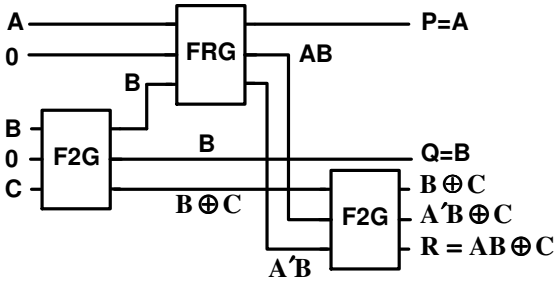


Fig. 4: Existing TG with parity preservation, presented in [11].

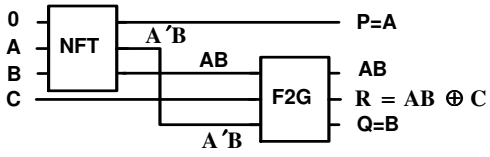


Fig. 5: Proposed parity preserving TG implementation using only two reversible gates

RESULTS AND DISCUSSION

Evaluation of the Proposed Parity Preserving Reversible TG: The proposed parity preserving reversible circuit is more efficient than the existing circuit presented in [11]. Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results in table 4.

Table 4: Comparative results of different parity preserving reversible Toffoli gate circuits

	This Work	Existing circuit[11]
No. of Gates	2	3
No. of Garbage Outputs	1	2
Total Clock Cycle	2	3
Total Logical Calculation	6α+3β+2δ	6α+4β+2δ

σ = Unit Clock Cycle
α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation

Comparing our proposed circuit with the existing circuit in [11], it is found that the proposed design approach requires only two reversible logic gates (one NFT gate and one F2G) but the existing design in [11] requires three reversible gates (one Fredkin Gate and two F2Gs). So, the proposed circuit is better than [11] in term of number of reversible logic gates, which is one of the main factors in reversible circuit design.

Garbage output is the output of the gate that is not used as a primary output or as input to other gate. One of the major constraints in designing a reversible logic circuit is to lessen number of garbage outputs. The proposed parity preserving reversible circuit produces only one garbage output, but the design in [11] produces two garbage outputs. So, we can state that our design approach is better than [11] in term of number of garbage outputs.

Another significant criterion in designing a reversible circuit is to minimize the number of required clock cycles. This work requires only two clock cycles. The existing design in [11] requires three clock cycles. So, we can state that our proposed parity preserving reversible circuit is better than the existing counterpart in term of number of required clock cycles.

One of the other main factors of a circuit is its hardware complexity. We can state that our proposed circuit is also better than [11] in term of hardware complexity.

Let
α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation
T= Total logical calculation

So, for [11] the Total logical calculation is: T=6α+4β+2δ, but for our proposed circuit, the Total logical calculation is: T=6α+3β+2δ. So, the proposed parity-preserving reversible circuit is also better than the existing circuit in term of complexity.

From the above discussion we can conclude that the propounded parity-preserving reversible circuit is better than the existing counterpart in all the terms. The synthesis methods using Toffoli gates are widely available. Thus, our proposed parity-preserving TG circuit can be used in designing fault tolerant reversible circuits.

CONCLUSION

In this research, we presented a novel 3-input 3-output reversible logic gate, NFT. It is a parity-preserving reversible logic gate. The gate NFT can be used for implementing arbitrary functions. It can implement all Boolean functions. We designed a parity preserving reversible TG circuit. Table 4 illustrates that the proposed fault tolerant reversible circuit is better than the existing counterpart. Furthermore, the restrictions of reversible circuits were highly avoided. The synthesis methods using Toffoli gates are widely available. Thus, our proposed parity-preserving TG circuit can be applied to the design of fault tolerant reversible circuits via simple substitution.

Synthesis of more parity-preserving reversible circuits are now being studied. We are also trying to minimize reversible circuits.

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