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The Research on Process Technology of SiGe/Si HBT

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Abstract. SiGe/Si HBT is a novel Si based device, compared with traditional BJT, SiGe/Si HBT has some advantages including high current gain, excellent frequency property and lower noise, energy band engineering and doping engineering introduced bring design freedoms. The fabricating basic process flow of SiGe/Si HBT is described, SiGe material epitaxial process, emitter mesa etching process, N type doping poly silicon and metal silicide fabricating process are studied, and the critical process control method are explored in the paper. The SiGe/Si NPN HBT of maximum current gain β=80 is fabricated by this process flow.

Keywords: SiGe/Si HBT; mesa structure; critical process

*1.Introduction

In 1957, H. Kroemer proposed heterojunction transistor structure with wide band emitter and narrow base band can improve the frequency characteristics of the transistor greatly [1]. From this theoretical point of view, SiGe technology has become research focus in Si filed, but SiGe material epitaxy is a prerequisite for its development. It is difficult for extension of the high quality stained SiGe alloy film with low defect density due to large mismatch rate of about 4.2% for Si and Ge lattice constant, useable SiGe film was successfully grown by MBE until 1984. Since then, SiGe alloy film epitaxial growth by chemical vapor deposition technology has been developed and it is the foundation for SiGe technology entering into commercial area. At present, SiGe material epitaxy technology consists of the whole wafer epitaxy, differential epitaxy, selective epitaxy. Whole wafer epitaxy is epitaxial growth of SiGe alloy layer on wafer with no pattern, the differential epitaxy and selective epitaxy are epitaxial growth of SiGe alloy layer on wafer with pattern, but there are differences between them. Poly SiGe can be epitaxial on the oxide layer for differential epitaxy, while it can't be epitaxial on the oxide layer for selective epitaxy. SiGe HBT manufacturing methods are divided into the following two by different epitaxial SiGe technology, SiGe mesa fabrication methods and SiGe planar structure fabrication methods. Compared with SiGe planar structure fabrication method, SiGe mesa structure fabrication method is simple, less process steps, and it can test the quality of materials quickly, therefore, SiGe material epitaxial process, emitter mesa etching process, N type doping poly silicon and metal silicide fabricating process of SiGe

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mesa structure fabrication process are studied and the critical process control method are explored in the paper.

2.Mesa SiGe HBT fabrication process

Figure 1 shows the polysilicon emitter SiGe HBT device structure, the main process is shown in Figure 2. Throughout the process, the emitter mesa etching will affect the emitter width and the outer base surface conditions directly, bad corrosion can cause junction leakage, N-type doped poly silicon and annealing process will affect the distribution of the emitter doping, and then affecting on the dc characteristics of device, different metal silicide has different contact resistance, it will affect RF characteristics of the device.

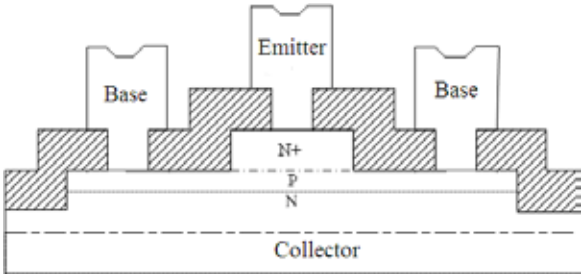


Fig 1. The profile of mesa SiGe HBT with Ploy silicon emitter

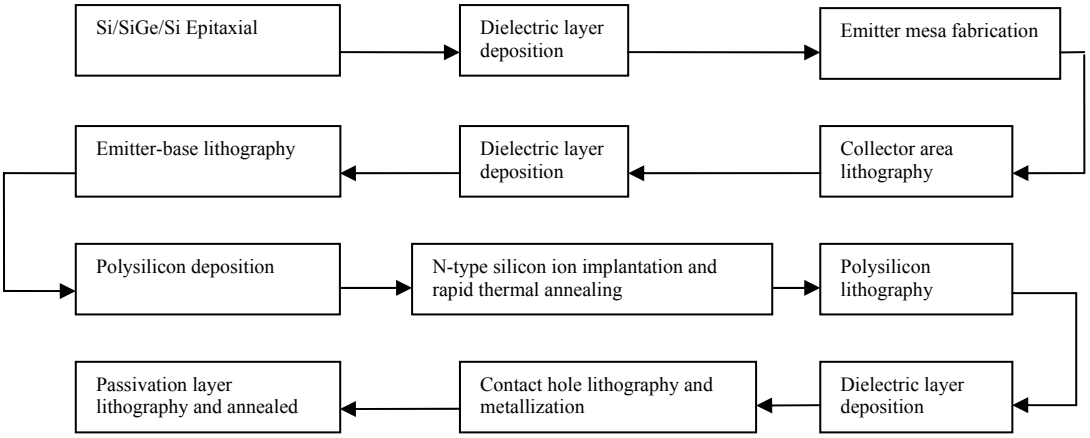


Fig 2. Process flow schematic diagram

3. Process of Poly-silicon Emitter Mesa SiGe HBT

At present, chemical vapor deposition is classified into ultra-high vacuum chemical vapor deposition, Reduce pressure chemical vapor deposition, low pressure chemical vapor deposition and rapid thermal chemical vapor deposition. We select low-pressure chemical vapor deposition to growth SiGe film, the reaction source consisted of SiH4 and GeH4, B2H6 as doping source , growth temperature at about 660 ℃, working pressure in 66.5Pa ~ 133Pa. Epitaxial process steps includes cleaning and deposition. Cleaning is divided into cleaning before entering into the furnace and in situ cleaning after entering into furnace, the first cleaning is to remove contamination and natural oxide layer, and the second cleaning is to remove the natural oxide layer sufficiently in H2 atmosphere, then deposition. The XRD analysis of

epitaxial wafer is shown in Figure 3. Si peak spectral is smooth and peak half-width is narrow, indicating that the Si lattice of the epitaxial materials is perfect. SiGe peak intensity is great and peak half-width is quite narrow. Clear pendelossung stripes between SiGe peak and Si peak shows the interface between SiGe and Si is straight and steep, which reveals that epitaxial film is fully strained.

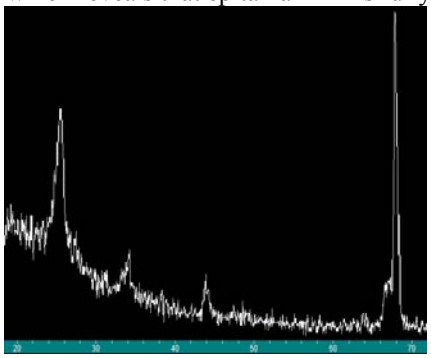


Fig 3.X-ray diffraction scan curves of epitaxial SiGe/Si wafer

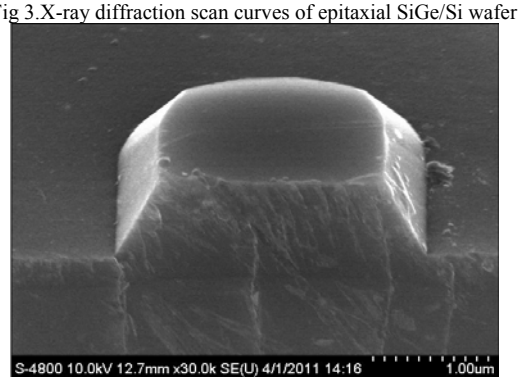
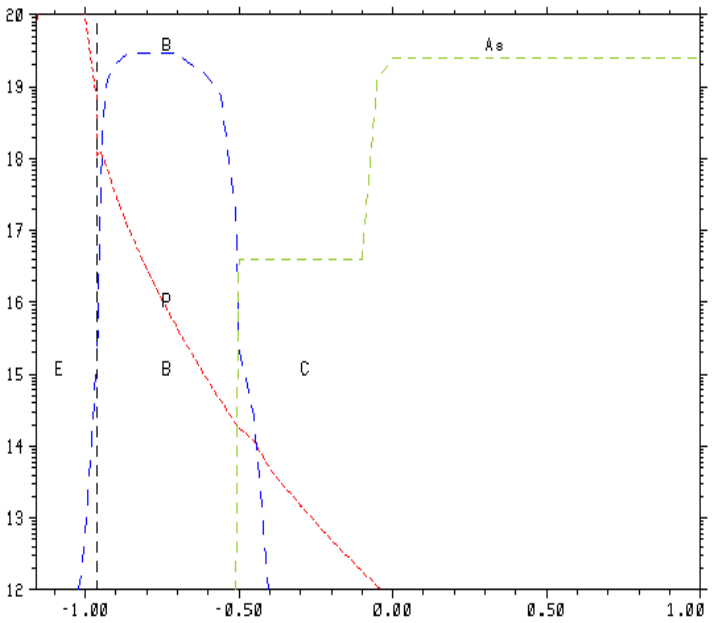
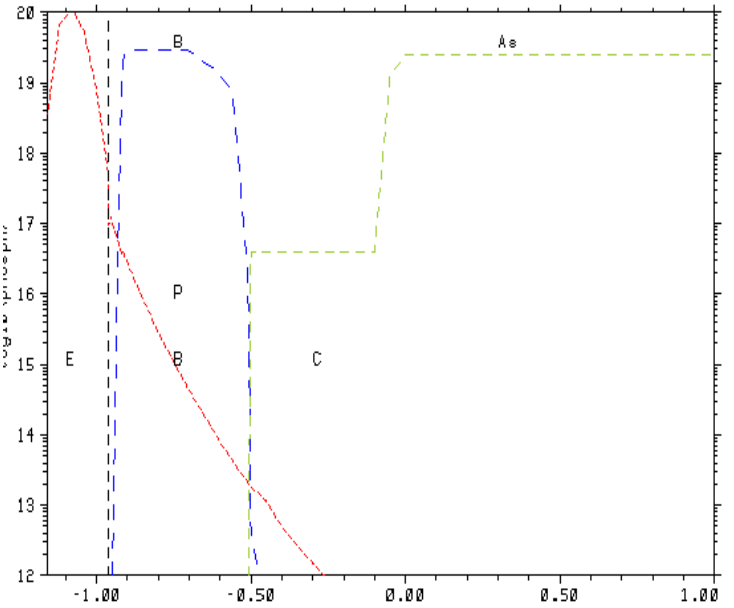


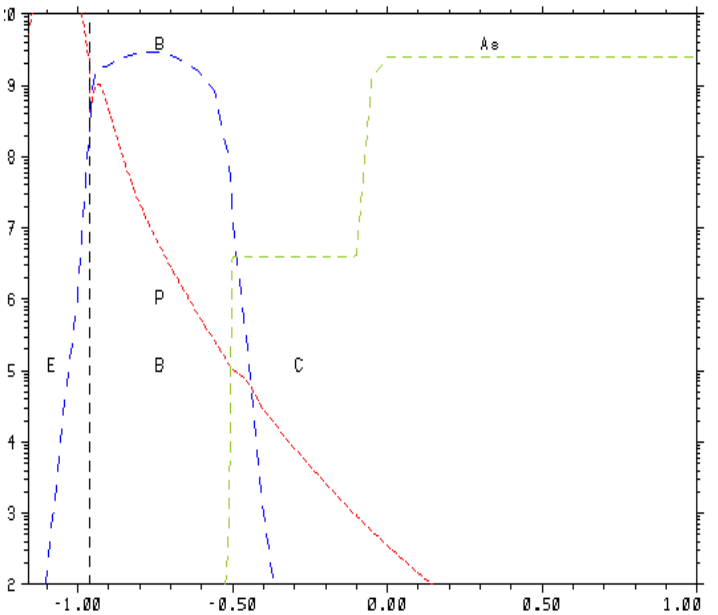
Fig 4. The etching results of <100> wafer



（a）Injection conditions 60kev 1E16



(b) Injection conditions 60kev 1E15



(c) Injection conditions 70kev 1E16

Fig 5. The result of implant simulation

In order to reduce the base transit time of Si / SiGe HBT, base is fabricated with only tens of nanometers, the etching velocity of dry etching is difficult to control and it is easy to damage extrinsic base surface, so wet etching is selected. The optimum wet etching technology is m(KOH):v(isopropanpol):v(H_2O)=6g:5ml:20ml, SiO_2 as masking film, wet etching temperature is 35℃, ultrasonic power is 100W, this process is described in detail in reference [2]. KOH pays a prime role in

chemical reaction, it is described by below chemical reaction equation: $Si+2KOH+H_2O=K_2SiO_3+2H_2\uparrow$, while H_2GeO_3 is one of the reaction between KOH and Ge, this production generates resultant which reduces reaction velocity by hydrolysis, the reaction velocity between SiGe and KOH is decreased due to existence of Ge. In addition, H_2 is one of production in the reaction between Si and KOH, while the reaction of Ge and KOH has not generated H_2, so we can determine the reaction ceasing or not by observing there is bubble on wafer surface or not. The etching result is shown in Fig4. As shown in Fig4, emitter mesa is steep and smooth, no corrosive defect, but section slopes due to anisotropic etching by KOH.

During fabrication of poly silicon emitter mesa SiGe HBT, poly silicon emitter fabrication is adding a layer of doped poly silicon, in terms of tunnelling theoretical model of interface oxide-like [3], there is a layer of oxide-like between mono-silicon and poly-silicon, the barrier generated by oxide-like layer is higher for hole than for electron. Hence, the tunnelling probability of hole is amaller than electron,base current decrease and electron implant efficiency increase by contraries. In addition, poly-silicon film can reduce surface recombination velocity of emitter, make the concentration distribution gradient of minority carriers decrease and is more conductive to increase electron implant efficiency. Compared with arsenic doped poly-silicon emitter, diffusivity of phosphorus is close to diffusive of boron, so it can prevent boron diffusing into emitter, and improve the breaking voltage. Sheet resistance of phosphorus doped poly-silicon decreases about 35% compared with arsenic doped poly-silicon[4], hence, selecting phosphorus as dopant. Concering implant conditions, the base doping is always 1E19-1E20, and emitter doping is always 1E18, taking into account charge storage, emitter capacitance, maximum current density and tunnelling current limitation. In order to determine optimum implant conditions, TSUPREM 4 process simulation software is taken[5], the simulation results are shown in Fig5. From Fig5, it can satisfy design requirements when implant energy is 60kev and dose is 1E16, emitter doping is 1E17 when implant energy is 60kev and dose is 5E15, while emitter doping is 1E19 when implant energy is 70kev and dose is 1E16, it is equivalent to base doping. In addition, SiGe alloy layer is sensitive to high temperature, in order to avoid high temperature conventional annealing process, RTA is taken for this process to activate implanted ion [6], the condition of RTA is 850℃,20S.

4.Conclusions

Fabrication of poly silicon emitter mesa SiGe HBT is realized by the key process below: LPCVD SiGe alloy layer epitaxial process, emitter mesa self-stopped etching process, phosphorus doping poly-silicon and RTA process, and metal salicide fabricating process, the critical process control method are explored, it builds the foundation for further preparation SiGe HBT with complicated structure.

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