Available online at www.sciencedirect.com
ScienceDirect
Neural Networks 21 (2008) 524–534
Neural Networks
www.elsevier.com/locate/neunet

2008 Special Issue

Compact silicon neuron circuit with spiking and bursting behaviour☆

Jayawan H.B. Wijekoon*, Piotr Dudek

School of Electrical and Electronic Engineering, The University of Manchester, United Kingdom

Received 8 August 2007; received in revised form 1 December 2007; accepted 14 December 2007

Abstract

A silicon neuron circuit that produces spiking and bursting firing patterns, with biologically plausible spike shape, is presented. The circuit mimics the behaviour of known classes of cortical neurons: *regular spiking* (RS), *fast spiking* (FS), *chattering* (CH) and *intrinsic bursting* (IB). The paper describes the operation of the circuit, provides simulation results, a simplified analytical model, and a phase-plane analysis of its behaviour. The functionality of the circuit has been verified experimentally. The paper introduces a proof-of-concept analogue integrated circuit, implemented in a 0.35 μm CMOS technology, and presents preliminary measurement results. The neuron cell provides an area and energy efficient implementation of the silicon cortical neuron, and could be used as a universal neuron circuit in VLSI neuromorphic networks that closely resemble the circuits of the cortex.

Keywords: VLSI; Cortical neuron; Neuromorphic; Firing pattern; Biomimetic circuit

1. Introduction

Cortical microcircuits are capable of performing sophisticated information processing, handling high computational throughput of sensory perceptions, cognitive processes, control and decision making with low energy consumption. The basic components of the cortical microcircuits are neuron cells. Mimicking their operation in silicon circuits is a subject of ongoing research interest (Bofill-i-Petit & Murray, 2004; Chicca et al., 2003; Indiveri, Chicca, & Douglas, 2006; Liu & Douglas, 2004; Merolla & Boahen, 2004; Tenore, Etienne-Cummings, & Lewis, 2004; Vogelstein, Mallik, & Cauwenberghs, 2004). It is hoped that analogue VLSI (Very Large Scale of Integration) models of neural circuits will provide very efficient brain emulation engines, and could potentially lead to the development of novel brain-inspired computer architectures.

It is an important consideration to design a neuron circuit with the least number of transistors and with least energy consumption, especially due to the fact such circuits are intended to be used in large-scale VLSI neural networks that consist of many thousands of neurons. When considering presently available neuron models the Integrate-and-Fire (I&F) neuron model is widely used due to its simplicity—typical I&F neuron cells use approximately 20 transistors to implement low power adaptive neuron circuitry (Indiveri, 2003; Schultz & Jabri, 1995). However, I&F neurons exhibit simple firing behaviour only—this might not be adequate for the development of VLSI circuitry which would be capable of imitating the processing of the cortex, which is made of a large number of more complex non-linear oscillatory neurons exhibiting a variety of inherent firing patterns. At a certain level of abstraction in modelling, it is important to account for this variety. Circuits implementing conductance-based neuron models (Hodgkin–Huxley type) have been reported in the literature (Mahowald & Douglas, 1991; Simoni & DeWeerth, 1999), however, these circuits consume a large number of transistors. The circuit implementations of oscillatory neuron models such as FitzHugh–Nagumo (Linares-Barranco, Sanchez-Sinencio, Rodriguez-Vazquez, & Huertas, 1991), Morris–Lecar (Patel & DeWeerth, 1997), Resonate-and-Fire (Nakada, Asai, & Hayashi, 2005), Hindmarsh–Rose (Lee et al., 2004) or Hardware Oregonator (Nakada, Asai, & Amemiya, 2004) use around 20 transistors. However, all these models do not accurately reproduce the shapes of the spikes that have been observed in the biological neurons and are also

☆ An abbreviated version of some portions of this article appeared in Wijekoon and Dudek (2007) as part of the IJCNN 2007 Conference Proceedings, published under IEE copyright.

* Corresponding author. Tel.: +44 161 3064714; fax: +44 161 3068946.
E-mail addresses: jayawan@ieee.org (J.H.B. Wijekoon), p.dudek@manchester.ac.uk (P. Dudek).

0893-6080/$ - see front matter © 2008 Elsevier Ltd. All rights reserved.
doi:10.1016/j.neunet.2007.12.037

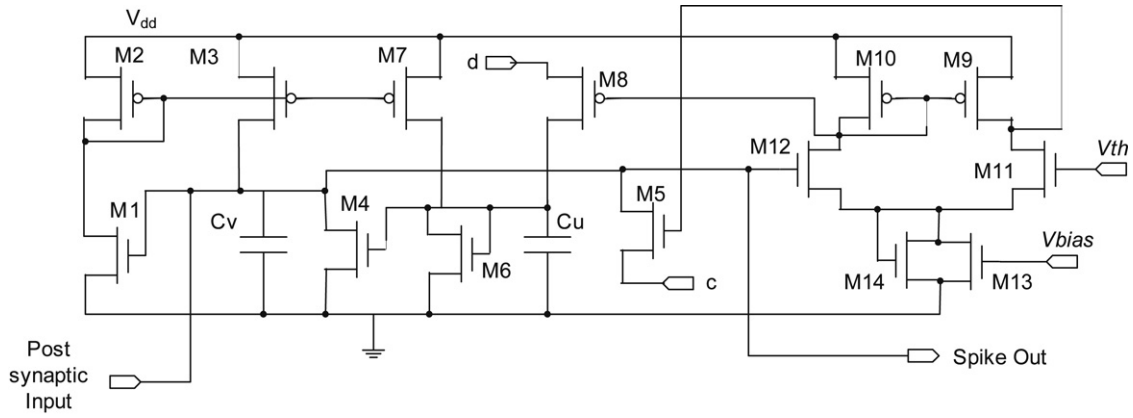

Fig. 1. The proposed cortical neuron circuit.

not capable of generating different types of spiking and bursting behaviour in a single circuit with tuneable parameters.

This paper elaborates the work published in Wijekoon and Dudek (2007). It presents a simple CMOS circuit model that exploits underlying non-linear characteristics of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) to implement the neuron using only 14 transistors. The spiking shape given by the circuit resembles that of real neurons. The circuit is capable of producing linear and non-linear responses (firing rate vs input current), with spike frequency adaptation, and a variety of spiking patterns such as regular spiking, fast spiking, low threshold spiking, intrinsic bursting, chattering etc.

2. Firing patterns of cortical neurons

Neurons in the cortex are found with great variety of dendritic morphology, ion channel distribution and composition. Hence, these neurons exhibit different electrical behaviour, transforming the same input signals into different firing patterns. A number of approaches to classifying neurons based on the electrophysiological recordings have been introduced (Connors & Gutnick, 1990; Markram, Toledo-Rodriguez, Wang, & Gupta et al., 2004; Nowak, Azouz, Sanchez-Vives, Gray, & McCormick, 2003; Petilla Convention, 2005; Toledo-Rodriguez, Gupta, Wang, Wu, & Markram, 2003). Many parameters, such as spike frequency, inter-spike-interval histogram, spike width, intra-burst frequency, adaptation index etc. can be used to classify the neurons. The basic classification used in this paper is given below.

The neuronal response to a step stimulus of supra-threshold current (post-synaptic input current that causes action potentials) displays either spiking or bursting firing behaviour. The spiking neurons are of two types: regular spiking (RS) and fast spiking (FS) (Nowak et al., 2003). The RS cells exhibit an *accommodation* (also known as *adaptation*) property: in a response to a supra-threshold current step they fire repeatedly, with a decreasing frequency, until the firing rate reaches a stable value, which depends on the input current. The RS cell class can be further sub-divided into two sub-types, the weak accommodating cells are called RS1 and strong accommodating cells are called RS2 (Toledo-Rodriguez et al., 2003). Examples of morphological cell that behave as RS1 type are neocortical layer II–VI *pyramidal cells*. The RS2 type cells are neocortical layer IV–VI *pyramidal cells* and *spiny stellate cells* (Connors & Gutnick, 1990).

The FS cells fire repetitively at high frequency with little or negligible accommodation to a sustained supra-threshold current injection. The action potentials of FS cells exhibit faster rise rate, fall rate and distinct fast after-hyperpolarisation (AHP) (Connors & Gutnick, 1990). Some neurons with FS behaviour commonly found in the cortex are, for example, neocortical *small basket cells*, *nest basket cells*, *bitufted cells* and *large basket cells* (Toledo-Rodriguez et al., 2003).

The basic bursting cell types are chattering (CH) and intrinsic bursting (IB) (Nowak et al., 2003). The CH neurons usually display repetitive long clusters of spikes to a sustained supra-threshold current injection. The IB neurons respond to a step current injection with a cluster of three to five initial spikes followed by an AHP, and then by either single spikes or burst at more or less regular intervals (Toledo-Rodriguez et al., 2003). These types are observed in sub-populations of *bitufted cells*, *bipolar cells* and *Martinotti cells* in the neocortex (Connors & Gutnick, 1990).

3. Proposed circuit

The circuit presented in this paper has been inspired by the mathematical neuron model proposed by Izhikevich (2003). That model attempted to provide a biologically realistic spike shape, using the simplest (from numerical computation point of view) set of mathematical equations. The required non-linear oscillatory behaviour is achieved using differential equations of two state variables and a separate after-spike reset mechanism. Our aim is to provide a similar, biologically plausible spike shape, using the simplest possible circuitry of the analogue VLSI implementation. We thus retain the basic form of the model formulae (Izhikevich, 2003), but use the non-linear functions readily available as device characteristics.

The proposed silicon cortical neuron circuit is shown in Fig. 1. The circuit contains 14 MOSFETs. The two state variables: "membrane potential" (V) and "slow variable" (U), are represented by voltages across capacitors C_v and C_u respectively. The circuit consists of three functional blocks: membrane potential circuitry (transistors M1–M5),

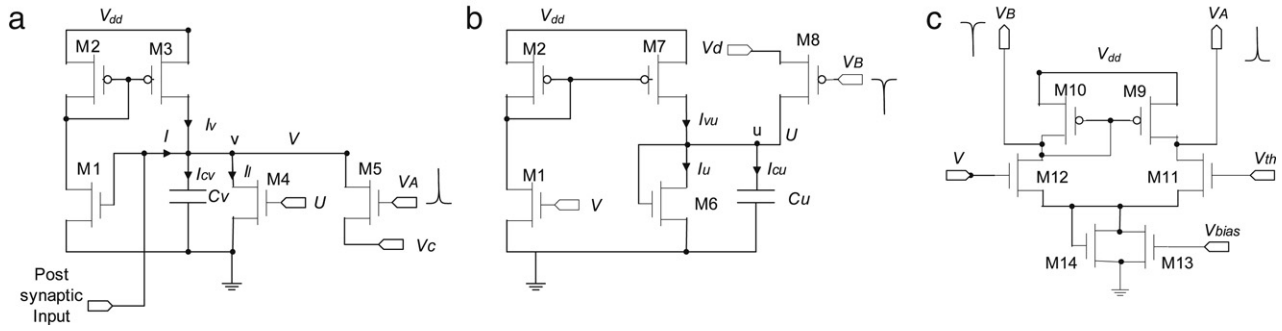

Fig. 2. Sub-circuits of the silicon cortical neuron: (a) Membrane potential circuit, (b) Slow variable circuit, (c) Comparator circuit.

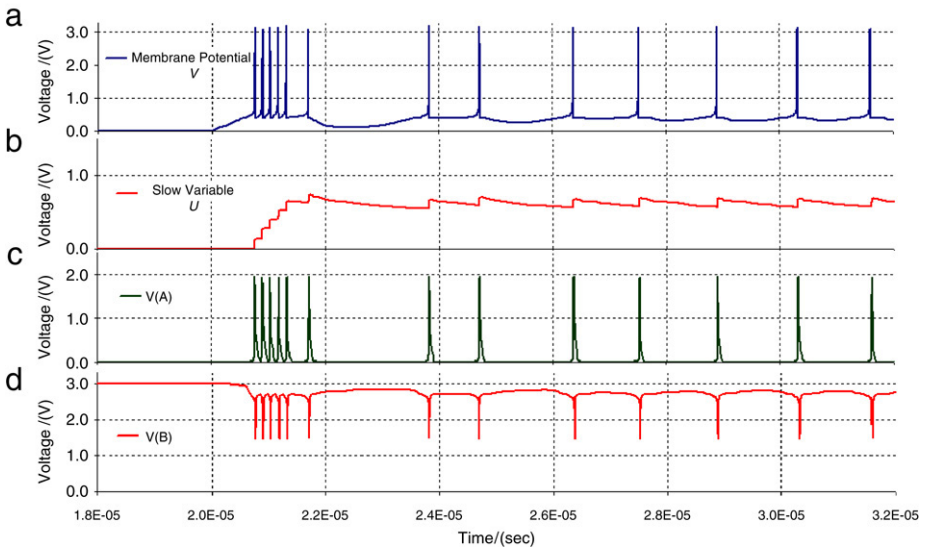

Fig. 3. Example waveforms of the membrane potential (V), slow variable (U) and the reset pulses (V_A and V_B).

slow variable circuitry (transistors M1, M2 and M6–M8) and comparator circuitry (M9–M14) as shown in Fig. 2(a), (b) and (c) respectively. Fig. 3 shows an example of how the key signals of the circuit (membrane potential, slow variable potential and resetting pulses) interact in order to provide an IB spike train. A qualitative explanation of circuit behaviour is given first, followed by a more detailed circuit analysis and simulation.

3.1. Membrane circuit

Fig. 2(a) illustrates the membrane potential circuit where the magnitude of the current through M3, I_v, is controlled by the membrane potential V. Transistors M2 and M3 form a current mirror circuit, with input current generated by M1. The current I_v acts as a positive feedback to generate spikes. The current I_l is the leakage current generated by M4 and the value of I_l is mostly controlled by the slow variable U. The current I is the post-synaptic input current (excitatory or inhibitory) and it is supplied by an external synapse. The net sum of these currents is integrated on the membrane capacitor C_v:

$$C_v \frac{\mathrm{d}V}{\mathrm{d}t} = I_v - I_l + I. \tag{1}$$

The membrane potential V evolves as given in Eq. (1) above. In particular, positive input current leads to the increase in V, which becomes more rapid as V increases, generating the spike. There is no explicit spike-generation threshold voltage, however, the process is affected by the slow variable U. The reset mechanism is implemented as follows. Once the spike is detected (by the comparator circuit) a pulse on V_A is generated. Consequently transistor M5 opens and membrane voltage is rapidly hyperpolarised. The transistor M5 size is designed so that the capacitor C_V is fully discharged during the V_A pulse, thus the value of V after-hyperpolarisation is entirely determined by the value set by the voltage V_c.

3.2. Slow variable circuit

The slow variable circuit is shown in Fig. 2(b). The magnitude of the current provided by M7, I_{vu} is determined by the membrane potential, in a way similar to the membrane circuit. (Transistors M2, and M7 form a current mirror circuit, with input current generated by M1). The transistors are scaled so that the drain current of transistor M7 is lower than that of M3 and capacitance value of C_u is selected as larger than that of C_v. This ensures that potential U will vary more slowly than V. The transistor M6 operates as a non-linear resistor and

the current through M6, I_u, is a function of the slow variable potential U. The net sum of these currents is integrated on the slow variable capacitor C_u:

$$C_u \frac{\mathrm{d}U}{\mathrm{d}t} = I_{vu} - I_u. \tag{2}$$

The slow variable, U evolves as given in Eq. (2) above. However, following a membrane potential spike, the comparator generates a pulse, V_B (as shown in Fig. 3(d)) to open the transistor M8. The narrow size of M8 and short duration of pulse V_B ensure that the capacitance C_u is not fully reset to V_d, but instead an extra amount of charge, controlled by V_d, is transferred onto C_u. Therefore each membrane spike provides a quick increase in the slow variable potential (as seen in Fig. 3(b)) which in turn increases the leakage current of the membrane potential and slows down the depolarisation after the spike. This mechanism is used, in particular, to provide the accommodation property of the spike train.

3.3. Comparator

The comparator circuit is shown in Fig. 2(c). The voltage V_{th} is the spike-detection threshold of the membrane potential. The voltage V_{bias} controls the bias current in the comparator. When the membrane potential increases above V_{th} the voltage at V_B is decreased and V_A is increased, generating reset signals. Due to the limited speed of the comparator and switches the reset is delayed, so the membrane potential V (in the membrane potential circuit) continues to increase beyond V_{th}, up to V_{DD}, but once V_A is increased, the membrane potential is reset to V_c which is lower than V_{th}. Consequently, voltages V_A and V_B return to their resting voltage level, completing reset pulses as shown in Fig. 3(c) and (d) respectively. The transistor M14 increases the comparator current during the spike, providing the required amplitude and duration of the reset pulse V_B.

4. Mathematical model

The behaviour of the circuit can be verified via numerical circuit simulations, which take into account detailed device models. However, useful insights can be obtained from circuit analysis using simplified first-order equations. Assuming long channel MOSFET devices, the following transistor model can be used:

$$|I_{ds}| = \begin{cases} 0 \quad \text{when } |V_{gs}| < |V_t| \\ \quad \text{(cut-off region)} & \text{(a)} \\ \mu C_{ox} \left(\frac{W}{L}\right)_M \left((V_{gs} - V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right) \\ \quad \text{when } |V_{gs}| > |V_t| \ \&\ |V_{ds}| < |V_{gs} - V_t| \\ \quad \text{(Linear region)} & \text{(b)} \\ \frac{1}{2}\mu C_{ox} \left(\frac{W}{L}\right)_M (V_{gs} - V_t)^2 \\ \quad \text{when } |V_{gs}| > |V_t| \ \&\ |V_{ds}| \geq |V_{gs} - V_t| \\ \quad \text{(Saturation region)} & \text{(c)} \end{cases} \tag{3}$$

where I_{ds} is the drain current of the transistor, V_{gs} is the gate–source voltage, V_{ds} is the drain–source voltage, V_t is the threshold voltage of the device, W is the gate width, L is the gate length, μ is the charge carrier mobility, and C_{ox} is the gate oxide capacitance per unit area.

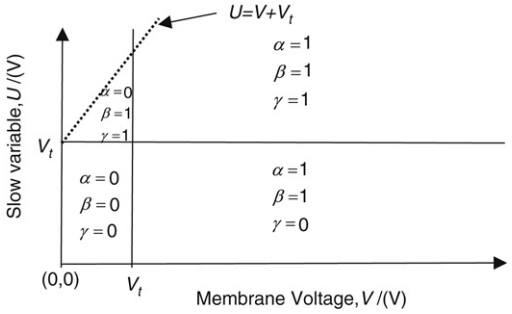

Fig. 4. Parameter values for Eqs. (4)–(6).

Using the above equation set of the MOSFET, the mathematical model of the proposed circuit can be deduced as follows (Wijekoon, 2007)

$$\dot{V} = \begin{cases} \frac{k}{C_v}\left\{\alpha\left[\frac{1}{2}\left(\frac{W}{L}\right)_{\text{M1}}(V - V_t)^2\right] \right. \\ \quad \left. - \beta\left[\frac{1}{2}\left(\frac{W}{L}\right)_{\text{M4}}(U - V_t)^2\right] + \frac{I}{k}\right\} \\ \quad \text{when } V \geq U - V_t & \text{(a)} \\ \frac{k}{C_v}\left\{\left(\frac{W}{L}\right)_{\text{M4}}\left((U - V_t)V - \frac{1}{2}V^2\right) + \frac{I}{k}\right\} \\ \quad \text{when } V < U - V_t & \text{(b)} \end{cases} \tag{4}$$

$$\dot{U} = \frac{k}{C_v}\left\{\alpha\left[\frac{1}{2}\left(\frac{W}{L}\right)_{\text{M1}}\left(\frac{L}{W}\right)_{\text{M2}}\left(\frac{W}{L}\right)_{\text{M7}}(V - V_t)^2\right] - \gamma\left[\frac{1}{2}\left(\frac{W}{L}\right)_{\text{M6}}(U - V_t)^2\right]\right\}. \tag{5}$$

$$\text{If } V > V_{th} \quad \text{then} \begin{cases} V \leftarrow V_c \\ U \leftarrow U + D \end{cases} \tag{6}$$

where, α, β and γ depend on V_t, V and U as given in Fig. 4. $k = \mu \times C_{ox}$ of the nMOSFETs and C_v and C_u are membrane and slow variable capacitance values respectively. The $(W/L)_{\text{M}x}$ is the gate width to length ratio of the MOSFET M_x. I is the post-synaptic current and V_c and D are externally tuneable parameters, where $D = f(V_d)$.

It should be noted that the '$V < U - V_t$' region of operation occurs sporadically. Simulations reveal that it only happens during a silent period after a burst of spikes in a CH type neuron. The Eq. (4)b provides a very slow increase in membrane voltage depending less on the variable U than V. This results in a lower inter-burst frequency. For the purpose of simplicity, however, Eq. (4)b can also be replaced by Eq. (4)a.

By selecting different values of (W/L) of transistors and capacitance values of C_u and C_v, diverse neural properties can be obtained (Wijekoon & Dudek, 2006). In the following analysis the following values are used $(W/L)_{\text{M1}} = 2.3/1$, $(W/L)_{\text{M2}} = 2.3/1$, $(W/L)_{\text{M4}} = 1.3/22$, $(W/L)_{\text{M6}} = 1.3/18$, $(W/L)_{\text{M7}} = 1.3/14$, $C_u = 1$ μF $C_v = 0.1$ μF and 0.35 μm CMOS process parameters: $k = 168\ \mu\text{AV}^{-2}$, $V_t = 0.5$ V. Using these values in Eqs. (4)–(6) in the MATLAB simulation environment, a variety of neural response types were obtained for various values of parameter V_C, as illustrated in Figs. 5 and 6.

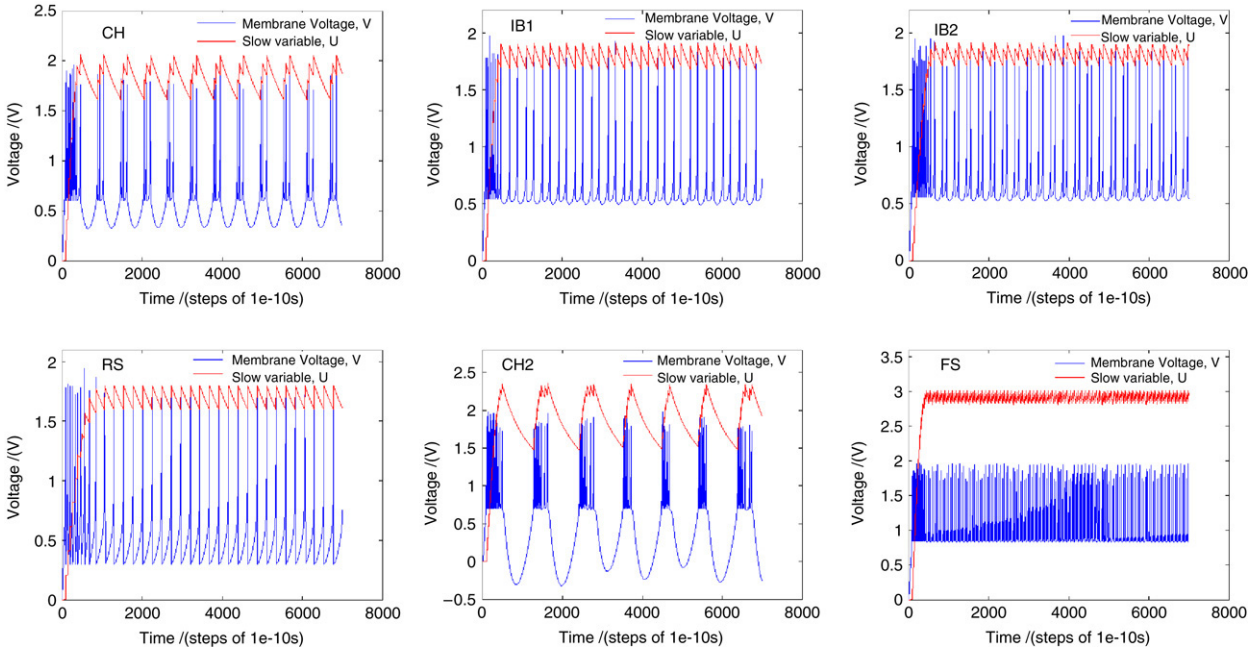

Fig. 5. The firing patterns obtained from the mathematical model derived from the proposed circuit: V_c values used to obtain these waveforms are given in Fig. 6.

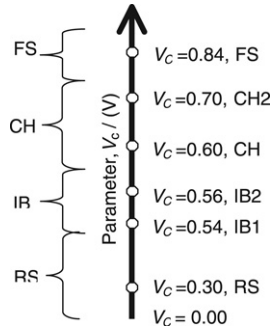

Fig. 6. The parameter space of the tuning variable V_c used to obtain different firing patterns shown in Fig. 5 ($V_d = 1.9$ V).

5. Phase-plane analysis

A phase plane analysis provides insight into the dynamics that take place in the circuit and facilitates the identification of circuit parameters directly related to a property of a spike or spike trains. The sequence of state points of the two variables (V, U) forms a trajectory in the 2D phase plane. The phase portrait can be drawn in the phase plane using the vector field of derivatives values $\mathrm{d}V/\mathrm{d}t$ and $\mathrm{d}U/\mathrm{d}t$, showing the direction in which the state variable evolves for any given state point in the phase plane. The set of points with $\mathrm{d}V/\mathrm{d}t = 0$ (i.e. *V-nullcline*) and $\mathrm{d}U/\mathrm{d}t = 0$ (i.e. *U-nullcline*) is important in identifying the dynamics of the system. The phase portrait, obtained using a SPICE simulation of the circuit, is shown in Fig. 7. The method used to obtain this plot is as follows. The comparator sub-circuit is removed from the circuit and two capacitors, C_u and C_v are replaced with two voltage-controlled voltage sources, with voltages U and V respectively. Currents through these sources, I_{Cu} and I_{Cv}, correspond to the total currents that would be charging/discharging the capacitances, as shown by Eqs. (1) and (2), i.e. they can be used to determine the derivatives of

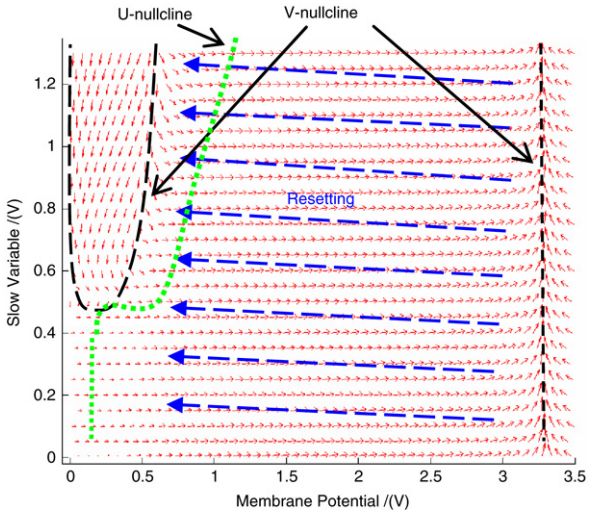

Fig. 7. Phase portrait of the proposed circuit with a 0.1 μA supra-threshold input current.

the state variables. Values of I_{Cu} and I_{Cv} are obtained from SPICE simulation for different sets of (U, V). These values are used to calculate the direction and magnitude of the vectors (log values of the vector magnitudes are plotted as arrows). As the phase portrait is obtained without the resetting operation, the direction of resetting is shown in Fig. 7 using dashed arrows.

5.1. Circuit operation

Consider the case when the circuit is biased so that it produces the CH firing pattern. When 0.1 μA post-synaptic current step is applied to the circuit, the phase-plane trajectories of the CH cell are shown in Fig. 8(a) and the time domain variations of the membrane potential and the slow variable

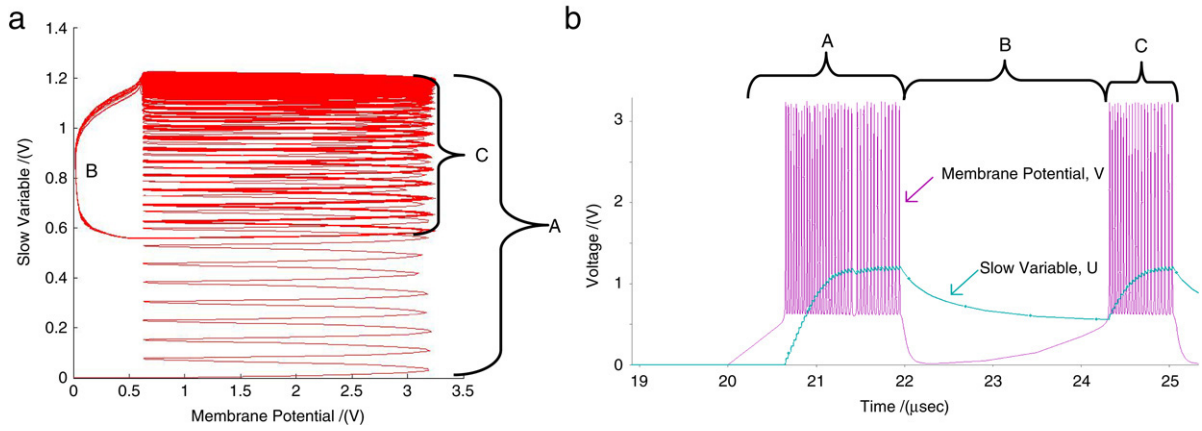

Fig. 8. Generation of the CH firing pattern: (a) State trajectory (b). Membrane potential and respective slow variable potential waveforms.

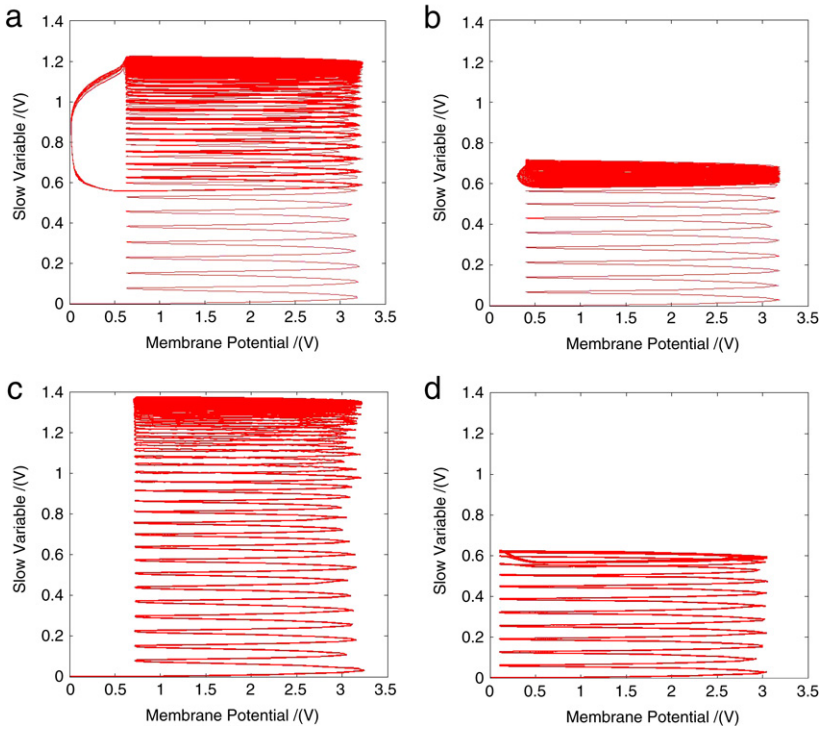

Fig. 9. State trajectories of (a) CH, (b) IB, (c) FS and (d) RS firing patterns.

potential are shown in Fig. 8(b). These plots have been obtained using a SPICE simulation of the full cortical neuron circuit.

As seen in Fig. 8(a), initially the membrane potential increases at a higher rate than that of the slow variable potential. At first it increases due to the input current, but beyond a certain value (for example, approximately 0.5 V in the example shown in the Fig. 8) the circuit's positive feedback results in the rapid increase of the membrane potential producing the rising edge of the spike. When the membrane potential reaches the spike-detection threshold V_{th}, this is detected by the comparator, which activates the resetting circuitry. The membrane potential reaches its maximum (≈3.2 V) before the reset pulse discharges the membrane to its resetting voltage (in this example $Vc \approx 0.6$ V). As $V_c < V_{th}$ this also deactivates the resetting circuit, completing one cycle of spike generation. The membrane starts increasing its potential again, repeating the dynamics of voltage building and resetting (this section is labelled as 'A' in Fig. 8(a) and (b)). Each spike also increases the slow variable potential U and the spiking continues until the variable U reaches a higher voltage so that the trajectory intersects the V-nullcline. When the V-nullcline is crossed, the orbit follows a new dynamic-route (Section 'B' in Fig. 8(a) and (b)) causing a fast discharge of the slow variable (AHP) until the trajectory reaches the U-nullcline where the rate of increase in V becomes dominant and significant. Once V becomes dominant, since the slow variable U is at a lower potential, it follows similar cycles as the initial Section 'A' but starting at a higher value (Section 'C'). These dynamics repeat as long as the supra-threshold current is sustained and the overall dynamics produce chattering behaviour. The dynamics of the initial phase

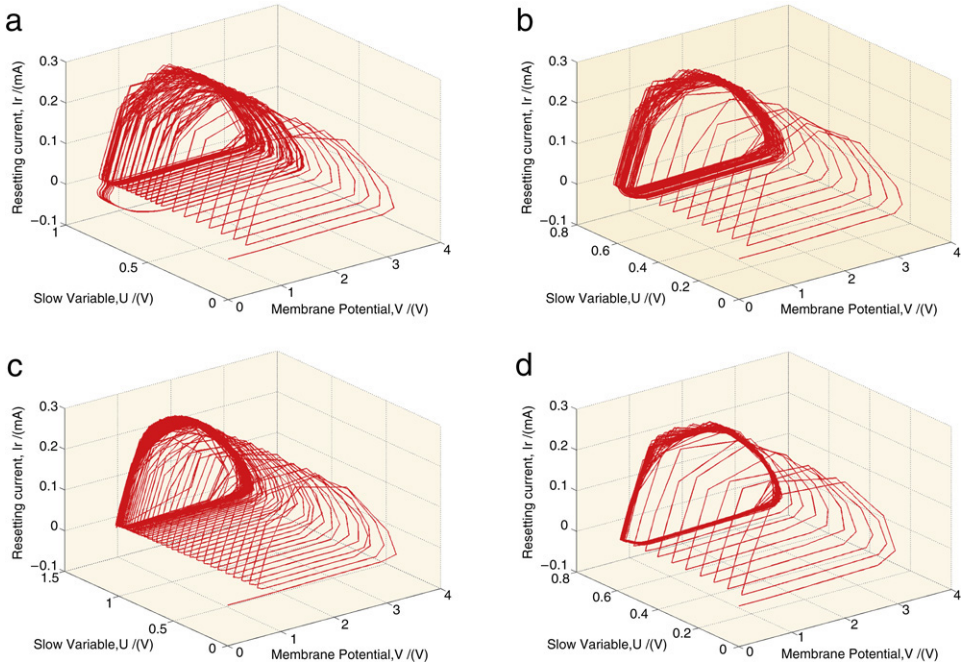

Fig. 10. 3D state trajectories of (a) CH, (b) IB, (c) FS and (d) RS firing patterns.

(Section 'A') are responsible for accommodation and the rest corresponds to the steady state dynamics. In a similar way, the IB, FS and RS neurons' trajectories and their dynamics can be explained from the figures shown in Fig. 9.

The system evolves with two state variables following Eqs. (4) and (5). However, in a practical circuit, the delayed resetting mechanism is more complex than the one expressed by Eq. (6), and can be analysed introducing an additional state variable. Hence the complete circuit operation can be represented clearly in a 3D geometry. The trajectories, where the resetting current (drain current of M5 in Fig. 1) has been used as the third state variable, are shown in Fig. 10.

6. Results

A VLSI chip containing 202 neurons with various circuit parameters (transistor sizes and capacitances) has been designed and fabricated in a 0.35 μm CMOS technology (CSI from Austria Micro-Systems) to experimentally verify the variation of neural properties with variation of the circuit parameters. The simulation and experimental results presented below are taken from a single neuron cell. The microphotograph showing the layout of a fabricated cell is shown in Fig. 11. This cell consumes 70×40 μm^2 silicon area and contains a neuron and its control and output buffer circuits.

The post-layout SPICE simulations of the circuit illustrate various types of cortical neuron firing patterns, obtained by changing the values of the voltages V_c, and V_d. Fig. 12 shows different responses of the circuit to a post-synaptic input current step of 0.1 uA; respective parameters of the tuning voltages V_c and V_d are provided in Fig. 13. The circuit parameters of this particular simulation are $(W/L)_{M1} = (2.3/1)$, $(W/L)_{M2} = (2.3/1)$, $(W/L)_{M3} = (2.3/1)$, $(W/L)_{M4} = (1.3/22)$, $(W/L)_{M5} = (5.3/1)$, $(W/L)_{M6} = (1.3/18)$, $V_{th} = 1.70$ V,

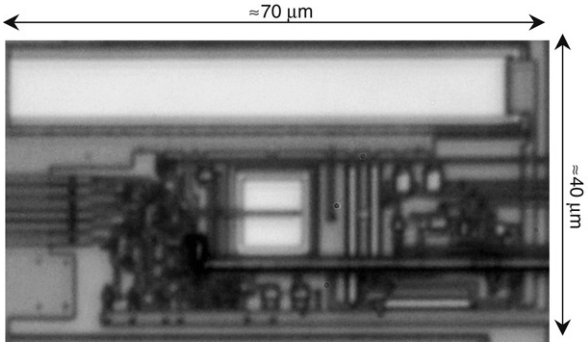

Fig. 11. Microphotograph of the fabricated neuron circuit with the control circuitry and output buffers.

$(W/L)_{M7} = (1.3/14)$, $(W/L)_{M8} = (1.3/1)$, $(W/L)_{M9} = (1/3.8)$, $(W/L)_{M10} = (1.8/1.3)$, $(W/L)_{M11} = (1/4.3)$, $(W/L)_{M12} = (2.8/1.3)$, $(W/L)_{M12} = (1.3/1)$, $(W/L)_{M13} = (2.3/3)$, $(W/L)_{M14} = (2.3/3)$, $V_{dd} = 3.3$ V, $V_{bias} = 0.6$ V, $C_v = 0.1$ pF and $C_u = 1$ pF. The typical mean (TM) technology parameter set was used.

Variations of firing patterns of selected CH, RS2, RS1, IB, LTS (Bacci, Rudolph, Huguenard, & Prince, 2003) and FS cell types with the variation of post-synaptic current step value are shown in Fig. 15.

It should be noted, that the firing patterns of VLSI neurons are on the microsecond scale rather than the millisecond scale of biological neurons. For comparative purposes, scaled time domain is considered in order to adopt biological classifications methods given in Nowak et al. (2003). The classification of spiking and bursting firing patterns using inter-spike-interval histograms obtained from the simulations was presented in Wijekoon and Dudek (2006). The RS neuron's spike frequency and the accommodation (spike frequency adaptation index) variation with the variation of the post-synaptic input

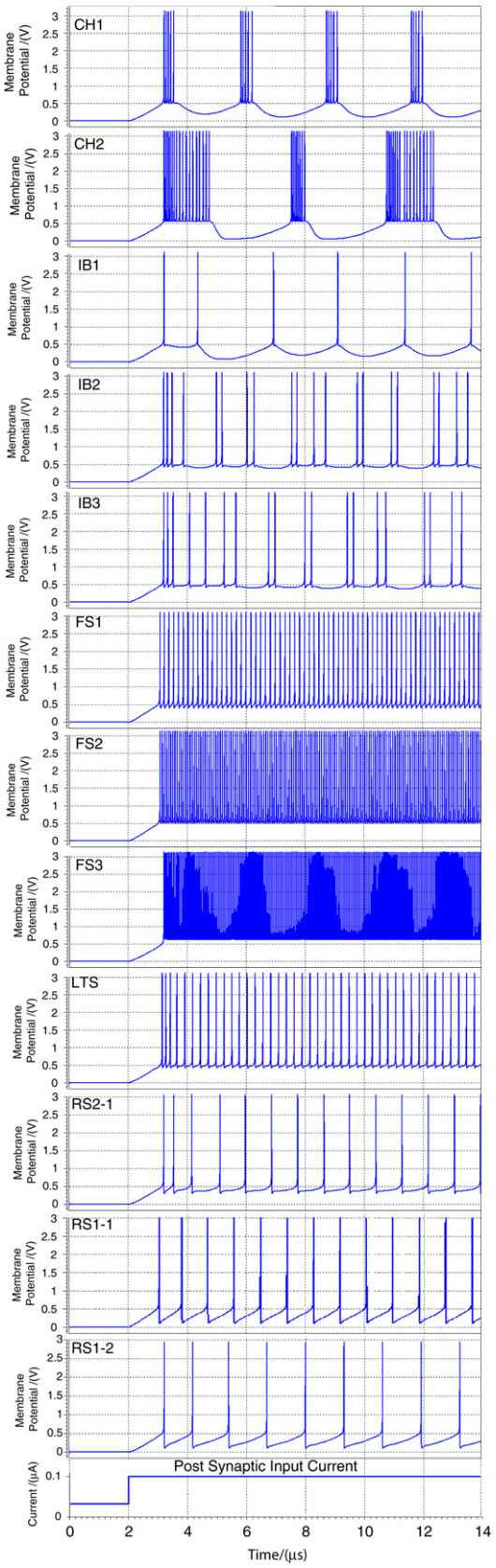

Fig. 12. Waveforms of CH, IB, FS, LTS and RS cells. Each plot shows voltage response of the proposed circuit to a 0.1 µA current step. Parameters V_c and V_d of each response are given in Fig. 13.

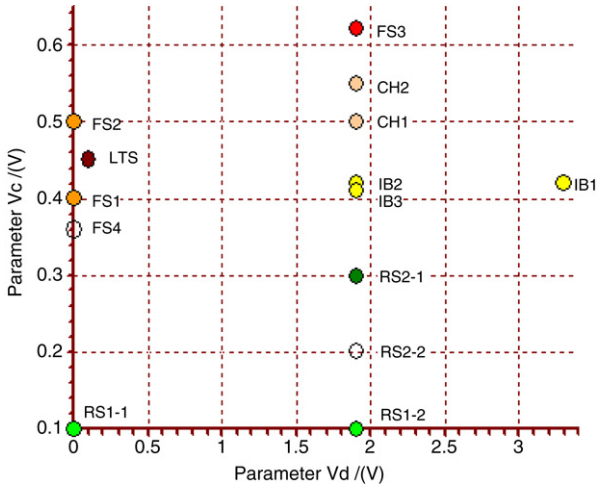

Fig. 13. Values of the parameters V_c and V_d which were used to obtain cortical neuron firing patterns shown in Figs. 12 and 15.

current were also provided in Wijekoon and Dudek (2006) which further illustrated the RS neuron's behavioural similarity with the biological RS neuron.

It is seen that some fast spiking continues even after the supra-threshold current is removed (Fig. 15(h) & (j)). However these cells shut off if the inhibitory post-synaptic current is provided. Bursts of three to five spikes are not present in IB1 patterns shown in Figs. 12 and 15(e). However, there are other points in the parameter space in which these bursts of three to five spikes train can be obtained. This is clearly seen in the experimental result in Fig. 16(b). Furthermore, by reducing the rate of slow variable (U) increase, either by increasing the C_u to C_v ratio (by changing the capacitance) or by reducing the flow of current to C_u (by increasing W/L of M6 or/and decreasing W/L of M7) produces more spikes in the initial burst if more flexibility is required. However, the flexibility of obtaining IB characteristics is somewhat limited, as they occur in a narrow range of tuning voltages, when compared with the other cell classes.

As seen in Figs. 12 and 15, different known types of cortical neurons are obtained using different values of V_c and V_d. It is also possible to obtain each type of neuron with different characteristics (frequency of spiking and accommodation), changing the width to length ratio of the transistors M4, M6 and M7 (Wijekoon & Dudek, 2006).

For practical implementations it is important to assess the robustness of the design with respect to process variability. As shown in Fig. 14, all firing patterns are obtainable by appropriate tuning of V_c across four process parameter corners: worst case power (WP), worst case one (WO), worst case zero (WZ) and worst case speed (WS).

Preliminary experimental test results obtained from a neuron cell in the fabricated VLSI chip are shown in Fig. 16. The waveforms were recorded using a digitising oscilloscope, from the output of the on-chip amplifier/buffer connected to the membrane potential of the neuron circuit fabricated with transistor sizes identical to the ones used in the simulations. The post-synaptic input current step was applied using an on-chip synapse (a single pMOS transistor), connected to a pulse

V_C /(V)	Corner analysis (worst case analysis)				
	WP	WO	TM	WZ	WS
0.00	RS2	RS2	RS1	RS1	RS1
0.10	RS2	RS2	RS1	RS1	RS1
0.20	IB	IB	RS2	RS1	RS1
0.30	CH	CH	RS2	RS1	RS1
0.40	CH	CH	IB	RS2	RS2
0.50	FS	FS	CH	RS2	RS2
0.60	FS	FS	CH	IB	IB
0.65	FS	FS	FS	CH	CH
0.70	-	-	FS	CH	CH
0.75	-	-	FS	FS	FS
0.80	-	-	-	FS	FS
0.90	-	-	-	FS	FS

Fig. 14. Effect of process variation on the value of V_c required to obtain various behaviours ($V_d = 1.9$ V).

generator. The voltages V_c and V_d are varied using external voltage sources, so that main types of characteristic firing patterns can be observed, as detailed in Fig. 16. Overall the experiments show a reasonable agreement with the simulations and it has been verified that the circuit is capable of generating all types of cortical neuron behaviour.

7. Comparisons of VLSI neurons

In order to provide a comparison between various VLSI neuron models, the number of MOSFETs used, the possibility of obtaining different spiking and bursting patterns, the pattern of the spike shape as compared with biological neurons and the power consumption of various circuits are listed in Table 1. Amongst these models, the proposed circuit is not only the simplest, but also most versatile in terms of its biologically plausible behaviour, and most energy efficient. It should be noted, that the power consumption figures depend on the number of spikes per second, and the technology used to implement these circuits. Furthermore, comparison is difficult due to absence of power consumption data in most of the literature. From the figures shown in Table 1, the I&F neuron in Indiveri (2003) appears to consume the least power, but its frequency of spiking is 100 Hz, much lower than the MHz spiking rate of the proposed circuit. Therefore energy per spike should be used as a figure of merit, as it provides a fair comparison of power consumption with respect to neuron's computational ability. This gives a 3–15 nJ energy consumption per spike for the I&F neuron circuitry (Indiveri, 2003) whereas the proposed compact silicon cortical neuron consumes only 8.5–9.0 pJ/spike.

8. Conclusion

We have presented a CMOS neuron circuit, which is capable of generating spiking and bursting firing behaviours, with a biologically plausible spike shape. The circuit behaviour has been verified via SPICE simulations and analysis of a simplified analytical model; and then confirmed through experiments with fabricated CMOS integrated circuits. The single circuit mimics most of the electrophysiological cortical neuron types and is capable of producing a variety of different behaviours, with diversity similar to that of real biological neuron cells. The behaviour of this universal cortical neuron cell can be adjusted using two external basing voltages. The circuit is implemented using 14 MOSFETS only, and consumes a small silicon area.

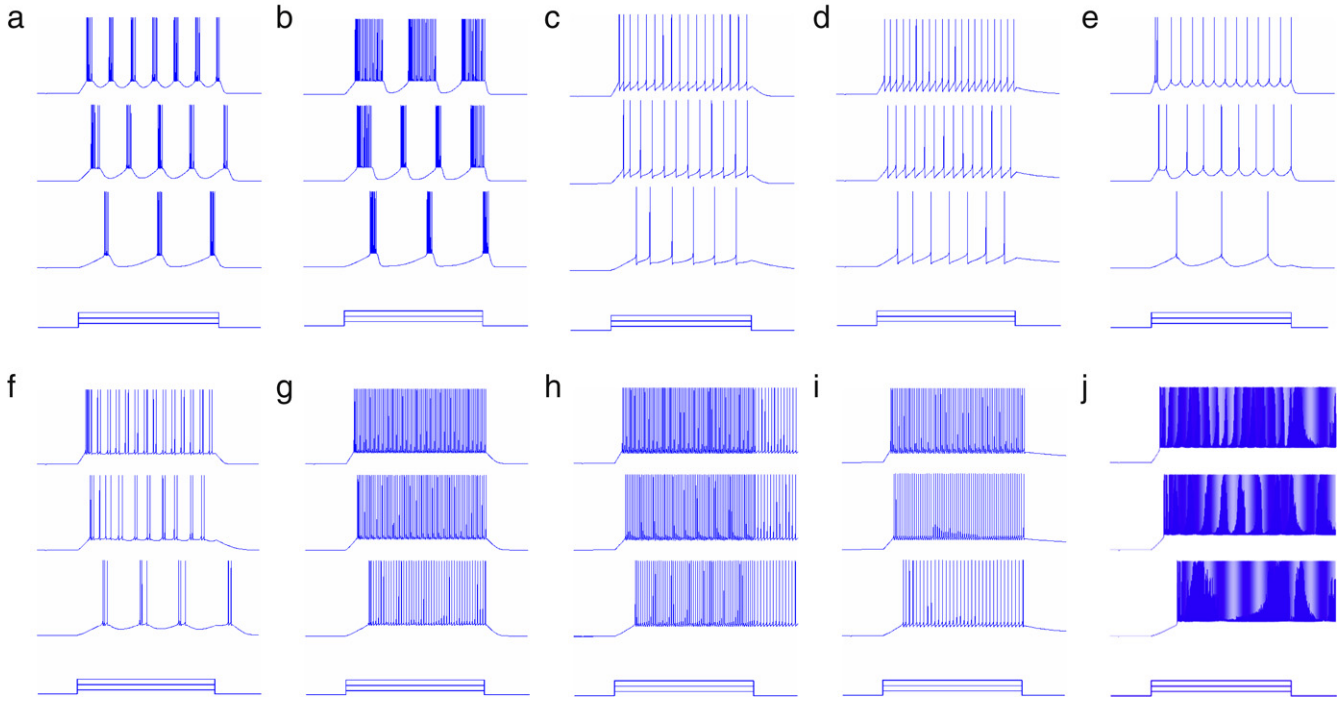

Fig. 15. Selected spiking and bursting firing pattern behaviour with the increase in step post-synaptic current (a) CH1, (b) CH2, (c) RS2-2, (d) RS1-1, (e) IB1, (f) IB2, (g) LTS, (h) FS1, (i) FS4 and (j) FS3. The respective *Vc* and *Vd* circuit parameters of these plots are given in the parameter space provided in Fig. 13. The plots shows responses to three increasing steps of dc-currents: 0.05 μA, 0.1 μA, and 0.15 μA except plot (b) is 0.05 μA, 0.1 μA, and 0.12 μA and plot (e) is 0.05 μA, 0.1 μA, and 0.25 μA.

Table 1
Comparison of the performances of the proposed neuron circuit and other VLSI neuron models

Neuron model	Approximate number of transistors used	Spiking and bursting (FS, RS,CH & IB)	Shape of the spike	Power (μW)	Reference
Conductance-based	27–30+	Simple spiking	Good	60	(Mahowald & Douglas, 1991)
Integrate-and-fire	18–20	Simple spiking	Fair	0.3–1.5	(Indiveri, 2003)
FitzHugh–Nagumo	21	Oscillatory	Envelope	–	(Linares-Barranco et al., 1991)
Morris–Lecar	22	Oscillatory	Envelope	–	(Patel & DeWeerth, 1997)
Resonate-and-Fire	20	Oscillatory	Pulse	–	(Nakada et al., 2005)
Hindmarsh–Rose	90	Bursting (CH)	Fair	163.4	(Lee et al., 2004)
Proposed circuit	14	*All the types*	*Good*	8–40	

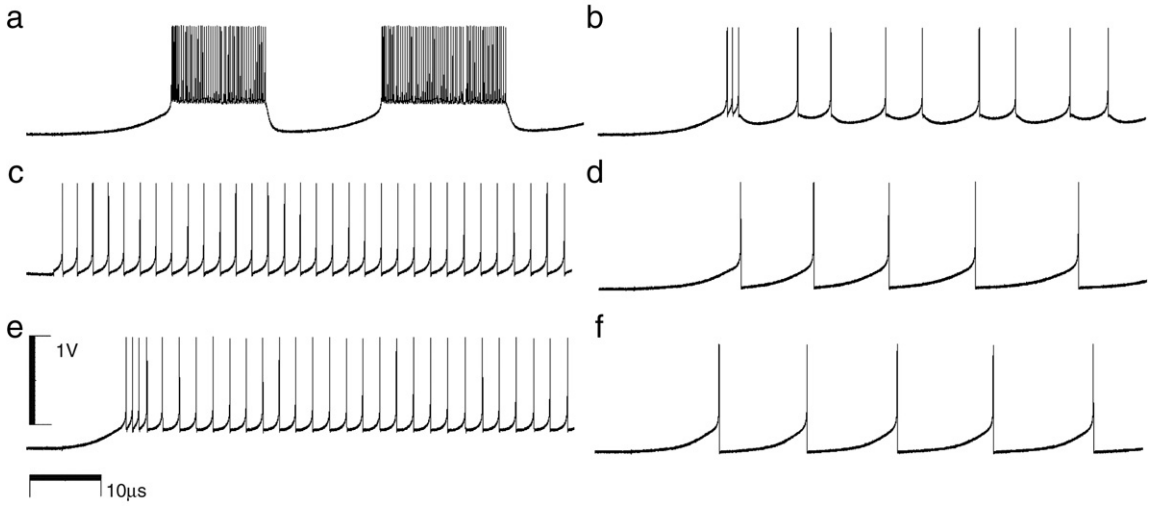

Fig. 16. Waveforms of experimental firing patterns obtained from a neuron circuit (waveforms are taken after the output buffer): (a) CH when $Vc = 0.6$ V, $Vd = 1.9$ V, (b) IB when $Vc = 0.5$ V, $Vd = 2.95$ V, (c) FS when $Vc = 0.45$ V, $Vd = 0$ V, (d) RS2 when $Vc = 0.2$ V, $Vd = 1.9$ V, (e) LTS when $Vc = 0.47$ V, $Vd = 0.07$ V, (f) RS1 when $Vc = 0.1$ V, $Vd = 0$ V. Each plot shows voltage response of the fabricated circuit to a 0.1 μA step current.

Furthermore, the energy consumption per spike is extremely low, making the circuit suitable for integration in large-scale massively parallel analogue VLSI systems implementing cortical microcircuits.

Acknowledgement

This work has been supported by the EPSRC, grant number EP/C010841.

References

Bacci, A., Rudolph, U., Huguenard, J. R., & Prince, D. A. (2003). Major differences in inhibitory synaptic transmission onto two neocortical interneuron subclasses. *Journal of Neuroscience*, *23*(29), 9664–9674.

Bofill-i-Petit, A., & Murray, A. F. (2004). Synchrony detection and amplification by silicon neurons with STDP synapses. *IEEE Transactions on Neural Networks*, *15*(5), 1296–1304.

Chicca, E., Badoni, D., Dante, V., D'Andreagiovanni, M., Salina, G., Fusi, S., et al. (2003). A VLSI recurrent network of integrate-and-fire neurons connected by plastic synapses with long term memory. *IEEE Transactions on Neural Networks*, *14*(5), 1297–1307.

Connors, B. W., & Gutnick, M. J. (1990). Intrinsic firing patterns of diverse neocortical neurons. *Trends in Neoscience*, *13*(3), 99–104.

Indiveri, G. (2003). A low-power adaptive integrate-and-fire neuron circuit. In *IEEE int. symp. circuits and systems* (pp. IV820–823).

Indiveri, G., Chicca, E., & Douglas, R. (2006). A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity. *IEEE Transactions on Neural Networks*, *17*(1), 211–221.

Izhikevich, E. M. (2003). Simple model of spiking neurons. *IEEE Transactions on Neural Networks*, *14*(6), 1569–1572.

Lee, Y. J. et al. (2004). Low power real time electronic neuron VLSI design using subthreshold technique. In *IEEE int. symp. circuits and systems: Vol. 4* (pp. IV-744–747).

Linares-Barranco, B., Sanchez-Sinencio, E., Rodriguez-Vazquez, A., & Huertas, J. L. (1991). A CMOS implementation of FitzHugh–Nagumo neuron model. *IEEE Journal of Solid-State Circuits*, *26*(7), 956–965.

Liu, S. C., & Douglas, R. (2004). Temporal coding in a silicon network of integrate-and-fire neurons. *IEEE Transactions on Neural Networks*, *15*(5), 1305–1314.

Mahowald, M., & Douglas, R. (1991). A silicon neuron. *Nature*, *354*(6354, 19–26), 515–518.

Markram, H., Toledo-Rodriguez, M., Wang, Y., Gupta, A., et al. (2004). Interneurons of the neocortical inhibitory system. *Nature Reviews Neuroscience*, *5*, 793–807.

Merolla, P., & Boahen, K. (2004). A recurrent model of orientation maps with simple and complex cells. In *Advances in neural information processing systems, vol. 16* (pp. 995–1002).

Nakada, K., Asai, T., & Amemiya, Y. (2004). Analog CMOS implementation of a bursting oscillator with depressing synapse. In *Proc. intelligent sensors, sensor networks and information processing conference* (pp. 503–506).

Nakada, K., Asai, T., & Hayashi, H. (2005). A silicon Resonate-and-fire neuron based on the volterra system. In *Int. symp. on nonlinear theory and its applications* (pp. 82–85).

Nowak, L. G., Azouz, R., Sanchez-Vives, M. V., Gray, C. M., & McCormick, D. A. (2003). Electrophysiological classes of cat primary visual cortical neurons in vivo as revealed by quantitative analyses. *Journal of Neurophysiology*, *89*, 1541–1566.

Patel, G. N., & DeWeerth, S. P. (1997). Analogue VLSl Morris-Lecar neuron. *Electronics Letters*, *33*(12), 997–998.

Petilla Convention, (2005). http://www.columbia.edu/cu/biology/faculty/yuste/petilla/petilla-webpages/petilla.html.

Schultz, S. R., & Jabri, M. A. (1995). Analogue VLSI 'integrateand-fire' neuron with frequency adaptation. *Electronic Letters*, *31*(16), 1357–1358.

Simoni, M. F., & DeWeerth, S. P. (1999). Adaptation in a VLSI model of a neuron. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, *46*(7), 967–970.

Tenore, F., Etienne-Cummings, R., & Lewis, M. (2004). A programmable array of silicon neurons for the control of legged locomotion. In *Proc. IEEE int. symp. circuits and systems* (pp. 349–352).

Toledo-Rodriguez, M., Gupta, A., Wang, Y., Wu, C. Z, & Markram, H. (2003). Neocortex: Basic neuron types. In M. A. Arbib (Ed.), *Hand book of brain theory and neural networks* (2nd ed.) (pp. 719–725). Cambridge, MA: MIT Press.

Vogelstein, R. J., Mallik, U., & Cauwenberghs, G. (2004). Silicon spike-based synaptic array and address-event transceiver. In *Proc. IEEE int. symp. circuits and systems* (pp. 385–388).

Wijekoon, J. H. B. & Dudek, P., (2007). Spiking and bursting firing patterns of a compact VLSI cortical neuron circuit. In *Int. join conf. on neural network* (pp. 1332–1337).

Wijekoon, J. H. B., (2007). Novel analogue VLSI circuit of a cortical neuron. *M.Phil. thesis*. School of Electrical and Electronic Engineering, The University of Manchester, UK.

Wijekoon, J. H. B. & Dudek, P., (2006). Simple analogue VLSI circuit of a cortical neuron. In *IEEE int. conf. on electronics, circuits and systems* (pp. 1344–1347).