Visualization of Crystalline Defects in Silicon, a Cause of Electrical Leakage in Semiconductor Devices

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Abstract – **Detection of electrical leakage in semiconductor devices indicates presence of electrical paths between junctions of p-doped and n-doped silicon, if no other physical abnormality is observed. This paper describes the use of advanced failure analysis tools to precisely locate and visualize crystalline defects in silicon that have caused electrical failure.**

I. Introduction

In n-doped silicon, crystalline defects such as dislocations, stacking faults, twins and precipitates, attract dopants, minority charge carriers that make transistors work, by creating recombination centers for dopants. In p-type silicon, crystalline defects show a donor-like behavior. This mechanism leads to formation of electrical leakage path, if a dislocation propagates across p-n junction of a device. With shrinking device sizes, even swallow dislocations are critical to electrical performance of the device.

To locate silicon crystalline defects by observation using optical microscope or scanning electron microscope (SEM), chemical delineation etching is required [1]. Chemical delineation etching is a process, that etchant preferentially attacks regions where dislocations intercepting the sample surface, creating visible geometric shapes, such as triangular, quadrilateral and circular etch pits. Chemical delineation etching, although being a useful method for determining crystalline defects density, distribution and orientation, it suffers drawback that physical visualization of crystalline defects is not possible especially for swallow, short-range crystalline defects since such defects may have already been etched away leaving behind perfect silicon crystal.

In this paper, we demonstrate the use of a combination of advanced failure analysis (FA) tools for direct visualization of crystalline defects in silicon that have caused electrical failure in transistors. Nanoprober has been proven to be capable of performing accurate electrical measurements with fewer artifacts. After accurate fault localization, transmission electron microscope (TEM) samples were prepared at appropriately selected cutting location to reveal crystalline defects. Direct visualization of crystalline defects plays an important role to exactly clarify failure mechanism, failure cause such that suitable and effective rectification actions may be proposed.

II. Experimental

Two cases are presented in this paper. In both cases, detection of leakage current and precise localization of defective site were carried out by Emission Microscope (EMMI) or nano-manipulator probing system. Failed sample was de-processed and SEM inspection using low accelerating voltage shows no physical abnormality at layers above substrate. It is suspected that leakage current is caused by silicon crystalline defects. Delayering processes and SEM inspection were carried out until only silicon remains.

Case I

A square underlying feature beneath the silicon surface was observed at defective site as shown in Fig. 1(a). Focused ion beam (FIB) milling across two parallel edges of the underlying square reveals cross-section of the defective site. Abnormal base profile of well was observed, showing a wavy dopant distribution profile, as shown in Fig. 1(b). The unusual base profile of well, however do no infer presence of electrical leakage path across the p-n junction. Cross-sectional TEM sample was prepared by using FEI Helios NanoLab 600i DualBeam across one of the remaining edges of the same underlying square, across unusual base profile of well.

There are obvious substrate dislocations at region of closed proximity to one of the edges of underlying square, at electrically failed site. The longest and deepest dislocation as observed in TEM image Fig. 2(a) has depth 4.8 µm from the substrate surface. High resolution TEM image shows regions of silicon having different crystalline orientation from bulk silicon (stacking fault), as shown in Fig. 2(b). Since depth of

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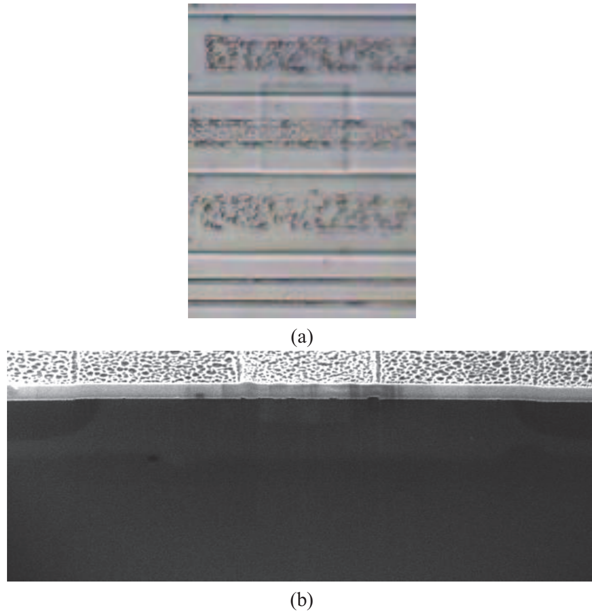
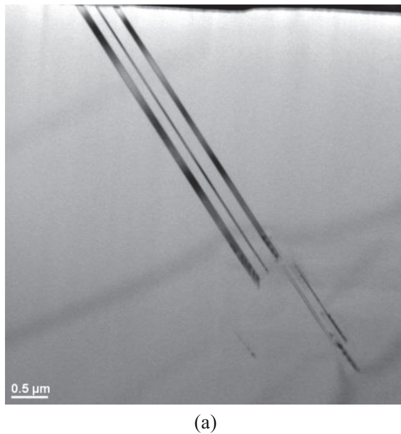
source/drain, as measured from the FIB cross-sectional image is 2.4 µm, the deepest reaching dislocation observed is long enough to span across p-n junction, forming leakage path across the source/drain and the well.



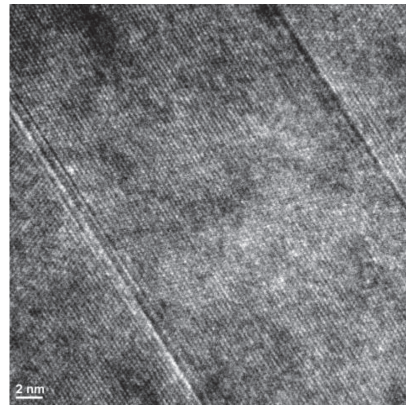
(a)

(b)

Fig. 1(a) Optical image of de-layered sample, a square feature underneath silicon surface was observed. (b) FIB cross-section image showing unusual base profile of well.



(a)



(b)

Fig. 2(a) TEM image shows substrate dislocations. (b) High resolution TEM image shows regions of different crystalline orientation.

Case II

Chemical delineation etching was performed on de-layered silicon-remaining only sample in another case. Two kinds of distinctive etch pits, triangular etch pits, and sink-in surfaces were observed on surface of the etched sample, as shown in Fig. 3. We believe these surface morphologies attribute to crystalline defect of different nature. A cross-sectional TEM sample was prepared across one of the edges of the sink-in surface. No substrate dislocation was found from TEM image. It is postulated that crystalline defect may have been completely etched during the chemical delineation etching, since precise control of etching time for crystalline defect of unknown depth is challenging, leaving behind only perfect silicon crystal.

To exactly clarify electrical failure mechanism, another defective sample, de-layered silicon remaining only sample, of the same device, was not subjected to chemical delineation etching. Defective region was identified by overlaying of circuitry and emission spot image. Two cross-sectional TEM samples were prepared along adjacent p-n junctions at region encompassed by the emission hot spot, as shown in Fig. 4. No crystalline defect was observed from one of the cross-sectional TEM samples prepared. Substrate crystalline defect, of depth about 3.2 um, was observed in the other cross-sectional TEM sample prepared, as shown in Fig. 5(a). Since the cross-sectional TEM sample was prepared along a p-n junction, also consider that the TEM lamella has a thickness of about 80 nm, chances of crystalline defect observed to span across p-n junction, causing electrical failure is high. Zoom-in image at the tip of defect shows stacking faults, as shown in Fig. 5(b).

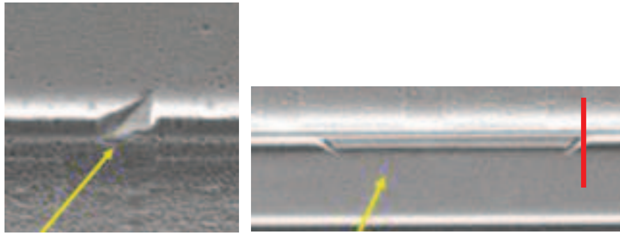


Fig. 3 Two kinds of etch pits observed on surface of silicon substrate after Secco etching. No crystalline defect was observed in cross-sectional TEM sample prepared at location indicated by red line of the etched sample.

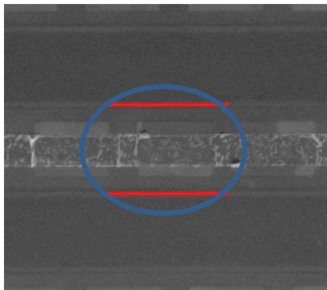
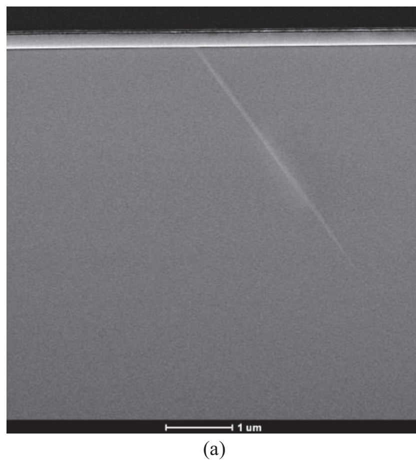
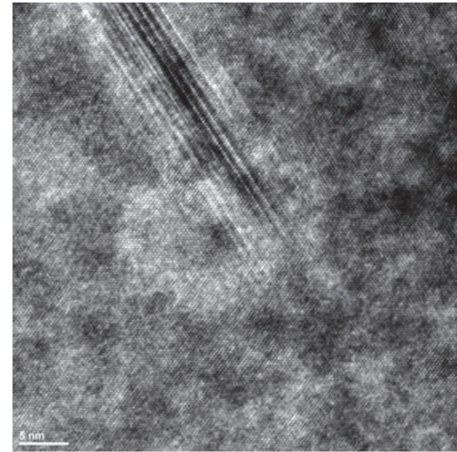


Fig. 4 Top-view image at defective site. Electrical hot spot was observed at region encompassed by the blue oval shape. Two cross-sectional TEM samples were prepared along adjacent p-n junction interfaces, as indicated by red lines.



(a)



(b)

Fig. 5 (a) STEM image of cross-sectional TEM samples prepared along one of the p-n junction interfaces, showing dislocation. (b) Zoom-in TEM image at tip of the same defect.

III. Discussion

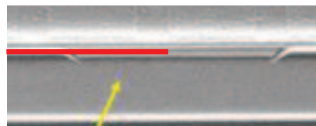
Crystalline defect observed in TEM sample without undergoing chemical delineation etching is correlated with etch pits observed in chemically etched sample. It is postulated that crystalline defect as observed in Fig. 5 would appear as triangular etch pit should the sample has undergone chemical etching. Width and depth of the triangular etch pit as observed in Fig. 3, is similar to the projected width from defect tip and the depth of crystalline defect observed in TEM image Fig. 5(a). The triangular etch pit spans across only one p-n junction, a likely explanation for absence of crystalline defect in cross-sectional TEM sample prepared along the other p-n junction.

It is postulated that crystalline defect that results in sink-in surface etched region, as shown in Fig. 3, comprises of silicon of different crystal orientation at sink-in and non-sink-in region. Schematically, bright field TEM image of the same type of un-etched crystalline defect would appear as Fig.6, being each side of diffraction contrast (bright and dark sides) representing one crystal orientation.

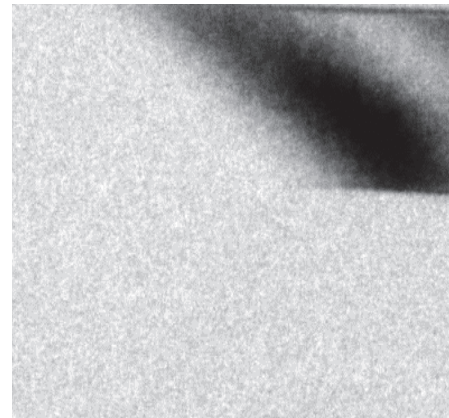
IV. Conclusion

Electrical characteristics of semiconductor devices can be directly or indirectly influenced by silicon crystalline defects. If crystalline defects span across p-n junction of device, it can increase leakage current to finally result in total electrical failure of the device. As transistor dimension shrinks, shallow short-range crystalline defects could affect electrical behavior of device. Locating and visualization of such shallow short-range crystalline defects gain increasing importance in

advanced semiconductor devices. Chemical delineation etching, although reveals silicon crystalline defects do not provide direct proof that such defects actually span across p-n junctions, causing electrical failure of device, since precise control of chemical etching time of crystalline defects of unknown depth is challenging. As such, capability to exactly clarify failure mechanism, to directly visualize silicon crystalline defects spanning across p-n junction, is crucial. Precise fault localization of electrical leakage site and appropriate choice of cross-sectional and planar TEM cutting location are crucial to the successful direct observation of silicon crystalline defects spanning across p-n junction. Once exact failure mechanism and failure cause have been clarified, possible cause of strain build-up in substrate can be postulated, suitable and effective rectification actions can be taken to improve the substrate quality, hence producing a high performance device [2, 3].



(a)



(b)

Fig. 6(a) Schematically, a cross-sectional TEM sample prepare at location indicated by red line, of a non-chemically etch sample, would appear as (b). Bulk silicon (light region) and silicon of different crystal orientation from bulk (dark region). Regions of different diffraction contrast in TEM image have different crystal orientation, and hence are chemically etched at a different rate.

References

[1] M. W. Jenkins, "A new preferential etch for defects in silicon crystals", *J. Electrochem. Soc.*, vol. 124, issue 5, pp. 757-762, 1977.

[2] Y. Igarashi, T. Yamaji and S. Nishikawa, "A new mechanism of failure in silicon p^+ /n junction induced by diffusion barrier metals", *Japanese Journal of Applied Physics*, vol.29, no.12, pp. L 2337 – L 2340, December 1990.

[3] J-C. Lin, Y-T. Hsu, C-K. Huang, W-C. Tsai and Y-H. Chou, "Investigation of substrate dislocation induced bit line soft failure", *Proceedings from the 30th International Symposium for Testing and Failure Analysis*, November 14-18, 2004 Worcester, Massachusetts.